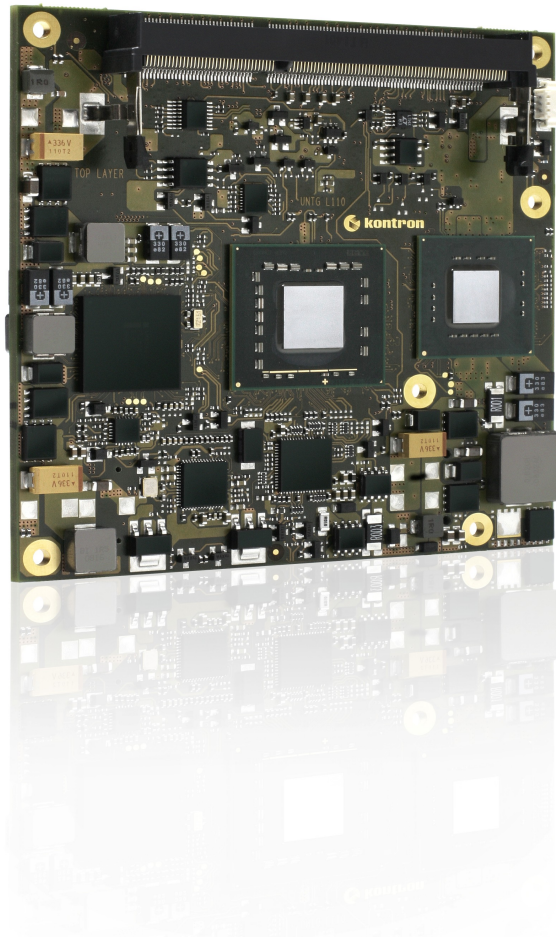


» Kontron User's Guide «



microETXexpress®-PC

Document Revision 1.1

» Table of Contents «

1	User Information.....	6
1.1	About This Document.....	6
1.2	Copyright Notice.....	6
1.3	Trademarks.....	6
1.4	Standards.....	6
1.5	Warranty.....	6
1.6	Technical Support.....	7
2	Introduction.....	8
2.1	Product Description.....	8
2.2	Naming clarification.....	8
2.3	Understanding COM Express™ Functionality.....	9
2.4	COM Express™ Documentation.....	9
2.5	COM Express™ Benefits.....	9
3	Specification.....	11
3.1	Functional Specification.....	11
3.2	Block Diagram.....	13
3.3	Mechanical Specification.....	14
3.4	Electrical Specification.....	14
3.4.1	Supply Voltage.....	14
3.4.2	Power Supply Rise Time.....	14
3.4.3	Supply Voltage Ripple.....	14
3.4.4	Power Consumption.....	14
3.5	Environmental Specification.....	15
3.5.1	Temperature.....	15
3.5.2	Humidity.....	15
3.6	MTBF.....	15
4	Connectors.....	17
4.1	Connector Location.....	17
4.2	Pinout List.....	18
4.2.1	General Signal Description.....	18
4.2.2	Connector X1A Row A.....	18
4.2.3	Connector X1A Row B.....	22
4.2.4	Connector X1B Row C.....	26
4.2.5	Connector X1B Row D.....	29
4.2.6	Alternative Pinout of HDMI.....	32
4.2.7	Alternative Pinout of Display Port.....	32
4.3	Signal Description.....	33
4.3.1	PCIexpress x1 lanes.....	33
4.3.2	USB.....	33
4.3.3	SATA.....	34
4.3.4	Audio.....	34
4.3.5	VGA Output.....	34
4.3.6	LVDS Flat Panel Interface (JILI).....	35
4.3.7	PCIexpress Graphics.....	35
4.3.8	SDVO.....	35

4.3.9	HDMI.....	35
4.3.10	Displayport.....	35
4.3.11	Ethernet.....	36
4.3.12	LPC.....	36
4.3.13	Power Control.....	36
4.3.14	Miscellaneous Circuits.....	37
5	Special Features.....	38
5.1	S5 Eco Mode.....	38
5.2	GPIO - General Purpose Input and Output.....	38
5.3	Usage of Different Graphic Interfaces.....	40
5.4	Speedstep Technology.....	42
5.5	Flash Backup Feature.....	42
5.6	Dynamic FSB Frequency Switching.....	44
5.7	Enhanced Intel Dynamic Acceleration Technology.....	44
5.8	VID-x.....	45
6	Design Consideration.....	46
6.1	Module Drillhole Dimension.....	46
6.2	Thermal Management.....	46
6.3	Heatspreader.....	47
6.4	Onboard Fan Connector.....	48
6.4.1	Location and Pinout of Fan Connector.....	48
6.4.2	BIOS Settings for Fan Control.....	49
6.4.3	Electrical Characteristics.....	49
7	System Ressources.....	51
7.1	Interrupt Request (IRQ) Lines.....	51
7.1.1	In 8259 PIC Mode.....	51
7.1.2	In APIC mode.....	51
7.2	Direct Memory Access (DMA) Channels.....	52
7.3	Memory Area.....	52
7.4	I/O Address Map.....	53
7.5	External Inter-IC (I2C) Bus.....	53
7.6	System Management (SM) Bus.....	53
7.7	JILI I2C Bus.....	53
7.8	SDVO I2C Bus.....	53
7.9	CRT I2C Bus.....	53
7.10	K-Station / JIDA32 resources.....	54
7.10.1	I2C.....	54
7.10.2	Storage.....	54
7.10.3	GPIO.....	54
7.10.4	Hardware Monitor.....	54
8	BIOS Operation.....	56
8.1	Determining the BIOS Version.....	56
8.2	Setup Guide.....	56
8.2.1	Start AMI® BIOS Setup Utility.....	56
8.3	BIOS Setup.....	58

- 8.3.1 Main Menu.....58
- 8.3.2 Module Info.....58
- 8.3.3 Advanced Menu.....61
- 8.3.4 PCIPnP Menu.....81
- 8.3.5 Boot.....82
- 8.3.6 Security.....83
- 8.3.7 Chipset.....84
- 8.3.8 Exit Menu.....89

- 9 Document Revision History.....90

1 User Information

1.1 About This Document

This document provides information about products from Kontron Embedded Modules GmbH and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

Copyright © 2003-2010 Kontron Embedded Modules GmbH

All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form or by any means (electronic, mechanical, photocopying, recording, or otherwise), without the express written permission of Kontron Embedded Modules GmbH.

DIMM-PC®, PISA®, ETX®, ETXexpress®, microETXexpress™, X-board®, DIMM-IO® and DIMM-BUS® are trademarks or registered trademarks of Kontron Embedded Modules GmbH. Kontron is trademark or registered trademark of Kontron AG.

1.3 Trademarks

The following lists the trademarks of components used in this board.

- » IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- » Microsoft is a registered trademark of Microsoft Corp.
- » Intel is a registered trademark of Intel Corp.
- » All other products and trademarks mentioned in this manual are trademarks of their respective owners.

1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at <http://www.kontron.com/support> for the latest product documentation, utilities, drivers and support contacts. Consult our customer section <http://emdcustomersection.kontron.com> for the latest BIOS downloads, Product Change Notifications and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 Product Description

Based on the COM Express™ standard, Kontron's microETXexpress®-PC, powered by a variety of Intel®'s Core2Duo® and CeleronM® processors, is a next-generation embedded module that brings advanced technology to tomorrow's applications, as well as continuing today's legacy devices. Built around serial differential signaling technologies, microETXexpress®-PC modules incorporate the following interfaces into 95 x 95 small form factor embedded module:

- » PCI Express, which provides a high performance I/O infrastructure with transfer rates starting at 2.5 Giga transfers per second over a x1 PCI Express lane
- » PCI
- » Serial ATA (SATA II)
- » USB 2.0
- » LVDS
- » High Definition Audio
- » Advanced Configuration and Power Interface (ACPI) for optimized power management

The microETXexpress®-PC is built around the Intel® Core™ Duo / Celeron® processor and the Intel® GS45 chipset. These modules feature the most current desktop features such as USB 2.0, SATA, and PCI Express buses.

The microETXexpress®-PC delivers up to 4GB on . For applications that require advanced real-time video capabilities, the microETXexpress®-PC has integrated graphics with 2D, 3D and Motion Video Acceleration and also supports PCI Express graphics, two SDVO ports or two HDMI capable DVI ports. Fast communications are possible courtesy of a Gigabit Ethernet port.

The microETXexpress®-PC supports up to 5 PCI Express x1 Lanes and PCI Express cards as well as established hardware solutions based on current buses such as 32-bit PCI. A Gigabit Ethernet port provides fast connectivity to LAN/WAN and 8 USB 2.0 ports provide fast and sufficient interfaces for external peripherals. microETXexpress®-PC modules also provide the following interfaces that are always located in the same physical position on each board:

PCI-express, PCI32, USB, serial ATA (SATA), parallel ATA (PATA), LVDS, as well as an ACPI (Advanced Configuration and Power Interface) for optimized power management. Mounting holes on the board provide secure mounting to allow the module increased shock and vibration resistance.

2.2 Naming clarification

COM Express™ defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component. Interfaces will provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the PCI bus and parallel ATA and PCI Express and Serial ATA.

- » ETXexpress® modules are Kontron's COM Express™ modules in basic form factor (125mm x 95mm)
- » microETXexpress® modules are Kontron's COM Express™ modules in compact form factor (95mm x 95mm)

- » nanoETXexpress® modules are Kontron's COM Express™ modules in the future ultra form factor (55mm x 84mm)

2.3 Understanding COM Express™ Functionality

All Kontron microETXexpress® and ETXexpress® modules contain two connectors; each of it has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D. On nanoETXexpress® modules only the primary connector Row A and Row B is used.

The primary connector (Row A and Row B) feature the following legacy-free functionality:

- » Ethernet
- » Serial ATA (SATA)
- » USB 2.0
- » LVDS/VGA and dual display video
- » High Definition Audio (Azalia)
- » LPC (low pin count) Bus
- » PCIexpress

2.4 COM Express™ Documentation

This product manual serves as one of three principal references for a COM Express™ design. It documents the specifications and features of microETXexpress®-PC. The other two references, which are available from your Kontron Support or from PICMG®, include:

- » The COM Express Specification defines the COM Express™ module form factor, pinout, and signals. This document is available from the PIGMG website by filling out the order form.
- » The COM Express™ Design Guide by PICMG serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express™ modules.



Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COM Express™ Benefits

Computer on modules express (COM Express™) modules are very compact, highly integrated computers. All (nano/micro)ETXexpress® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each (nano/micro)ETXexpress® module is based on connector type 1 or 2 of the COM Express™ specification. This standardization allows designers to create a single-system baseboard that can accept present and future (nano/micro)ETXexpress® modules.

(nano/micro)ETXexpress® modules include common personal computer (PC) peripheral functions such as:

- » Graphics
- » USB ports
- » Ethernet
- » Sound
- » SATA

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETXexpress®, microETXexpress® and nanoETXexpress modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of a COM Express™ solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express™ baseboard can work with several successive generations of COM Express® modules.

A COM Express™ baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specification

3.1 Functional Specification

Processor: Intel® Core™ Duo / Celeron®

CPU:	SP9300 (2x2.26GHz, 25W TDP) SL9400 (2x1.86GHz, 17W TDP) SU9300 (2x1.2GHz, 10W TDP) CM722 (1,2GHz 5.5W TDP) CM723 (1.2GHz, 10W TDP)
Cache:	1MB / 3MB / 6MB

Chipset Memory Controller Hub: Intel® GS45

Speed:	800/1066 MHz
RAM:	Single Channel up to 1 x DDR3 SO-DIMM
PEG:	One x16 PCIe port for PCI Express based graphic cards

Chipset IO Controller:

USB:	8 x USB 1.1/2.0
Audio:	HD Audio
PCI Express:	5 PCIe X1(6 PCIe X1 without LAN)
PCIe x4 mode:	YES, PCIe lanes #0 - #3
PCI Bus:	PCI Rev 2.3 (33MHz/3.3V) with 4 external PCI Masters

Integrated Graphics: Intel® GMA X4500MHD (Gen5.5)

Graphics Memory:	1024MB
Graphics Core Render Clock:	320MHz in Low Performance Mode 533MHz in High Performance Mode
Memory Bandwidth (GB/s):	17
API:	10 / 2.1
Pixelpipelines:	10
Pixelshader:	4.0
Hardware accelerated:	MPEG2, VC-1, AVC, Blue-Ray Support

Display Interfaces

Simultaneous Display:	2
CRT max Resolution:	QXGA (2048x1536)
LVDS Bits/Pixel:	1x18, 2x18
LVDS Bits/Pixel with dithering:	1x24, 2x24
LVDS max Resolution:	UXGA (1600x1200)
PWM Backlight Control:	YES
TV out:	YES
HDTV support:	480i/p, 576i/p, 720p, 1080i/p
Digital Display Interfaces:	2 x SDVO / HDMI /DP
SDVO connection:	Multiplexed with PEG
SDVO HDCP support:	HDCP 1.2 (Keys optional)



HDMI and Display Port don't support embedded audio in current revisions.

Storage

IDE interface:	JMD330 SATA#3 to PATA (IDE Master only)
SATA interfaces:	3 x SATA 300 (SATA#0-2; SATA#3: Sata2Pata)
SATA AHCI features:	NCQ, HotPlug, Staggered Spinup, eSATA, PortMultiplier
SATA RAID features:	0, 1
onboard SSD:	NO
SD Card support:	NO

Connectivity

Ethernet:	10/100/1000 Mbit
Ethernet controller:	Intel® 82567 (Boazman)
LAN boot:	YES

additional Interfaces

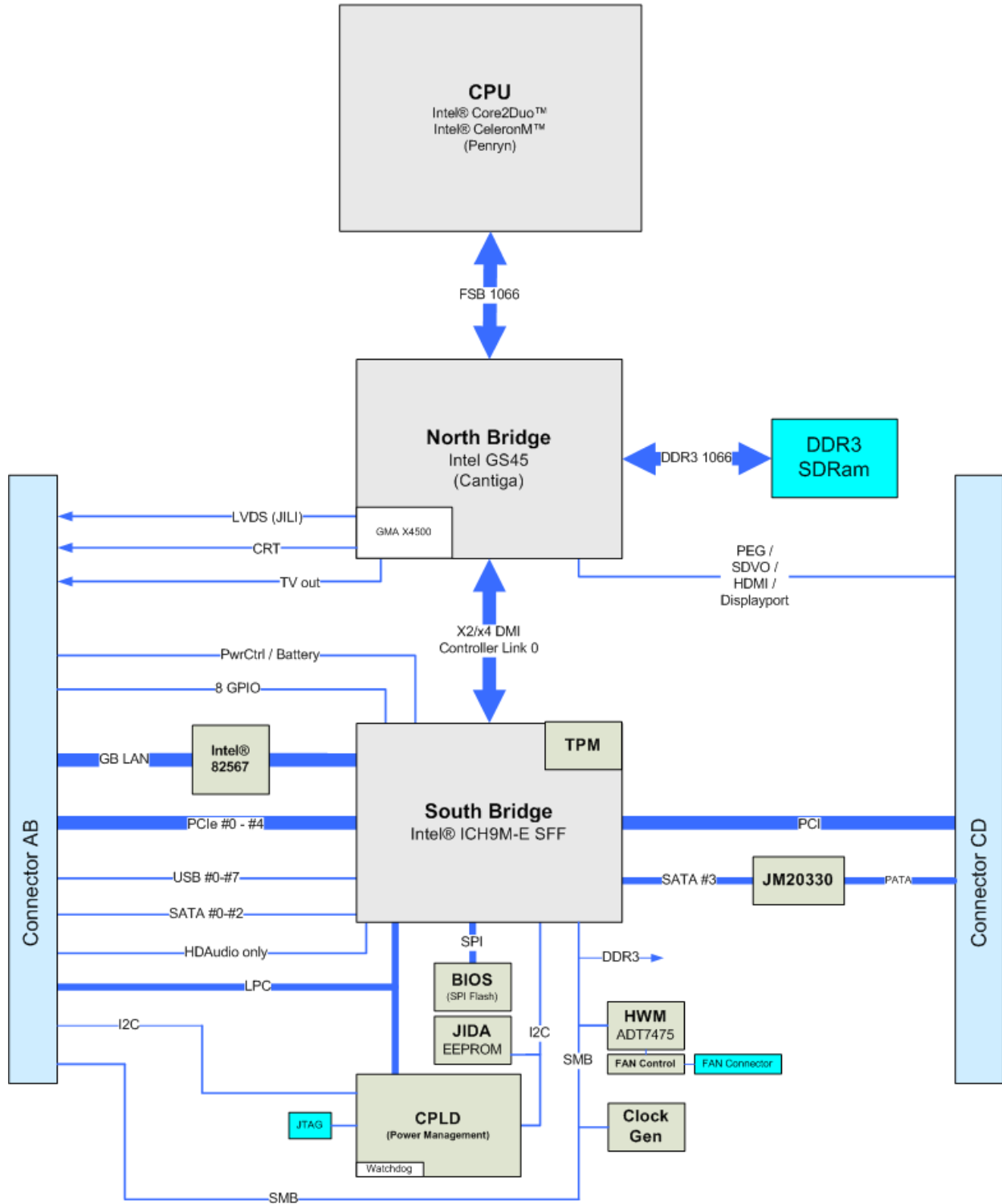
Audio	HD Audio
Trusted Platform Module	iTPM 1.2 (integrated in ICH9M)

Kontron Features

I2C support:	Fast I2C
MARS support:	Extended
JIDA / EAPI support:	JIDA 16/32
K-Station:	YES
JILI support:	Extended
Flash Backup:	YES
S5 Eco Mode:	YES
Darkboot / Bootlogo support:	YES
Watchdog support:	YES

3.2 Block Diagram

microETXexpress®-PC



3.3 Mechanical Specification

Dimension

- » 95.0 mm x 95.0 mm (3.75" x 3.75")
- » Hight approx. 12mm (0.4")

3.4 Electrical Specification

3.4.1 Supply Voltage

nominal Voltage:	12V +/- 5%
Wide Range input:	8.5V - 18V
5V_Stb:	5V DC +/- 5%



If a module is E1 rated and should be used in E1 temperature range the supply voltage must be 12V +/- 5%!

3.4.2 Power Supply Rise Time

- » The input voltages shall rise from $\leq 10\%$ of nominal to within the regulation ranges within 0.1ms to 20ms.
- » There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

3.4.3 Supply Voltage Ripple

- » Maximum 100 mV peak to peak 0 – 20 MHz

3.4.4 Power Consumption

The maximum Power Consumption of the different microETXexpress®-PC modules is between 14 - 43W (100% CPU load; 90°C CPU temperature). Further details with measurements and TDP values of the single variants can be found in our [customer section](#). Information there is available after registration.

3.5 Environmental Specification

3.5.1 Temperature

With Kontron Embedded Modules GmbH heatspreader plate assembly

Operating:

- » Ambient temperature: 0 to +60 °C
- » Maximum heatspreader-plate temperature: 0 to +60 °C

Non-operating: -30 to +85 °C



The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Without Kontron Embedded Modules GmbH heatspreader plate assembly

Operating:

- » Maximum operating temperature: 0 to +60 °C

Non operating: -30 to +85 °C



The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

3.5.2 Humidity

- » Operating: 10% to 90% (non condensing)
- » Non operating: 5% to 95% (non condensing)

3.6 MTBF

The following MTBF (Mean Time Before Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The Telcordia calculation used is "Method 1 Case 3" in a ground benign, controlled environment (GB,GC). This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned in.

Other environmental stresses (extreme altitude, vibration, salt water exposure, etc) lower MTBF values.

System MTBF (hours): 1754488 @ 40°C

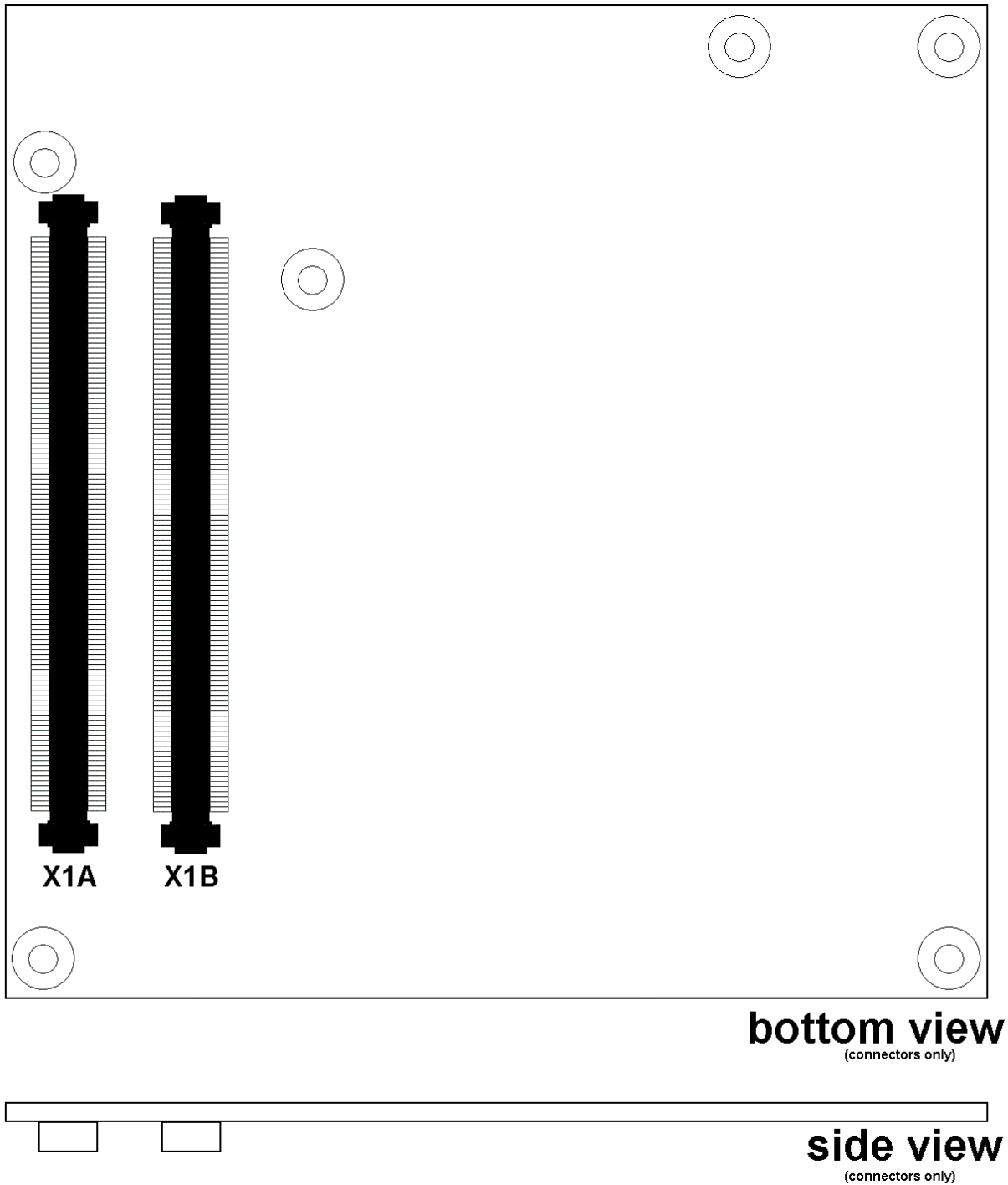


Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4 Connectors

The pinouts for microETXexpress®-PC Interface Connectors X1A and X1B are documented for convenient reference. Please see the COM Express™ Specification and COM Express™ Design Guide for detailed, design-level information.

4.1 Connector Location



4.2 Pinout List

4.2.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection



To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.2.2 Connector X1A Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	GBE0_MDI3_N ; Ethernet Receive Data -	DP-I	-	-
A3	GBE0_MDI3+	GBE0_MDI3_P ; Ethernet Receive Data -	DP-I	-	-
A4	GBE0_LINK100#	GBE0_LINK100# ; Ethernet Speed LED	0-3,3	-	-
A5	GBE0_LINK1000#	GBE0_LINK1000# ; Ethernet Speed LED	0-3,3	-	-
A6	GBE0_MDI2-	GBE0_MDI2_N ; Ethernet Receive Data -	DP-I	-	-
A7	GBE0_MDI2+	GBE0_MDI2_P ; Ethernet Receive Data -	DP-I	-	-
A8	GBE0_LINK#	GBE0_LINK# ; LAN Link LED	OD	-	-
A9	GBE0_MDI1-	GBE0_MDI1_N ; Ethernet Receive Data -	DP-I	-	-
A10	GBE0_MDI1+	GBE0_MDI1_P ; Ethernet Receive Data +	DP-I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	GBE0_MDI0_N ; Ethernet Transmit Data -	DP-0	-	-
A13	GBE0_MDI0+	GBE0_MDI0_P ; Ethernet Transmit Data +	DP-0	-	-
A14	GBE0_CTREF	GBE0_CTREF	0-1,8	-	is on a power rail controlled by Intels ME
A15	SUS_S3#	PM_SLP_S3_EXT#	0-3,3	PU 10k 3,3V (S5)	-
A16	SATA0_TX+	opt. SATA_TX0_P ; SATA 0 Transmit Data +	Nc	-	-
A17	SATA0_TX-	opt. SATA_TX0_N ; SATA 0 Transmit Data -	Nc	-	-
A18	SUS_S4#	PM_SLP_S4_EXT#	0-3,3	-	-
A19	SATA0_RX+	opt. SATA_RX0_P ; SATA 0 Receive Data +	Nc	-	-
A20	SATA0_RX-	opt. SATA_RX0_N ; SATA 0 Receive Data -	Nc	-	-
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA_TX2_P ; SATA 2 Transmit Data +	DP-0	-	-
A23	SATA2_TX-	SATA_TX2_N ; SATA 2 Transmit Data -	DP-0	-	-
A24	SUS_S5#	PM_SLP_S#5	0-3,3	-	-
A25	SATA2_RX+	SATA_RX2_P ; SATA 2 Receive Data +	DP-I	-	-
A26	SATA2_RX-	SATA_RX2_N ; SATA 2 Receive Data -	DP-I	-	-
A27	BATLOW#	PM_BATLOW# ; Battery Low	I-3,3	PU 8k25 3,3V (S5)	-
A28	ATA_ACT#	ATA_LED# ; SATA LED	0-3,3	PU 10k 3,3V (S0)	int. PU 15k in ICH9 only active if

					PLTRST#=0
A29	AC_SYNC	HDA_SYNC ; HD Audio Sync	0-3,3	-	opt. for x4: PU 1k 3,3V(S0)
A30	AC_RST#	HDA_RST# ; HD Audio Reset	0-3,3	-	int. PD 20k in ICH9
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	HDA_BITCLK ; HD Audio Clock	0-3,3	-	int. PD 20k in ICH9 active only in S3
A33	AC_SDOUT	HDA_SDOUT ; HD Audio Data	0-3,3	-	int. PD 20k in ICH9- x4 ⇒ PU 1k 3,3V(S0)
A34	BIOS_DISABLE#	BIOS_DISABLE#	I-3,3	-	-
A35	THRMTRIP#	EXT_THRMTRIP#	I/O-3,3	PU 10k 3,3V (S0)	-
A36	USB6-	USB6_N ; USB Data - Port6	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A37	USB6+	USB6_P ; USB Data + Port6	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A38	USB_6_7_OC#	USB_67_OC# ; USB OverCurrent Port 6/7	I-3,3	PU 10k 3,3V (S5)	-
A39	USB4-	USB4_N ; USB Data - Port4	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A40	USB4+	USB4_P ; USB Data + Port4	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB2_N ; USB Data - Port2	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A43	USB2+	USB2_P ; USB Data + Port2	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A44	USB_2_3_OC#	USB_23_OC# ; USB OverCurrent Port 2/3	I-3,3	PU 10k 3,3V (S5)	-
A45	USB0-	USB0_N ; USB Data - Port0	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A46	USB0+	USB0_P ; USB Data + Port0	DP-I/O	-	int. PD 15k in ICH9 ; 5V tolerant
A47	VCC_RTC	V_BAT	PWR 3V	-	-
A48	EXCDO_PERST#	EXCDO_PERST#;Express card reset	0-3,3	-	-
A49	EXCDO_CPPE#	EXCDO_CPPE# ; capable c. request	I-3,3	PU 10k 3,3V (S5)	-
A50	LPC_SERIRQ	LPC_SERIRQ ; Serial Interrupt Request	IO-3,3	PU 10k 3,3V (S0)	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	opt. PCI Express lane 5 + Transmit	Nc	-	just available if no GbEthernet PHY is used.
A53	PCIE_TX5-	opt. PCI Express lane 5 - Transmit	Nc	-	just available if no GbEthernet PHY is used.
A54	GPIO	EXT_GPIO ; General Purpose Input 0	I-3,3	PU 10k 3,3V (S0)	-
A55	PCIE_TX4+	PCI Express lane 4 + Transmit	DP-0	-	-
A56	PCIE_TX4-	PCI Express lane 4 - Transmit	DP-0	-	-

A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 + Transmit	DP-0	-	-
A59	PCIE_TX3-	PCI Express lane 3 - Transmit	DP-0	-	-
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 + Transmit	DP-0	-	-
A62	PCIE_TX2-	PCI Express lane 2 - Transmit	DP-0	-	-
A63	GPI1	EXT_GPI1 ; General Purpose Input 1	I-3,3	PU 10k 3,3V (S0)	-
A64	PCIE_TX1+	PCI Express lane 1 + Transmit	DP-0	-	-
A65	PCIE_TX1-	PCI Express lane 1 - Transmit	DP-0	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	EXT_GPI2 ; General Purpose Input 2	I-3,3	PU 10k 3,3V (S0)	-
A68	PCIE_TX0+	PCI Express lane 0 + Transmit	DP-0	-	-
A69	PCIE_TX0-	PCI Express lane 0 - Transmit	DP-0	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_A_DATA0_P ; LVDS Channel A Data0+	DP-0	-	-
A72	LVDS_A0-	LVDS_A_DATA0_N ; LVDS Channel A Data0-	DP-0	-	-
A73	LVDS_A1+	LVDS_A_DATA1_P ; LVDS Channel A Data1+	DP-0	-	-
A74	LVDS_A1-	LVDS_A_DATA1_N ; LVDS Channel A Data1-	DP-0	-	-
A75	LVDS_A2+	LVDS_A_DATA2_P ; LVDS Channel A Data2+	DP-0	-	-
A76	LVDS_A2-	LVDS_A_DATA2_N ; LVDS Channel A Data2-	DP-0	-	-
A77	LVDS_VDD_EN	LVDS_VDD_EN ; LVDS Panel Power Control	O-3,3	PD 100k	-
A78	LVDS_A3+	LVDS_A_DATA3_P ; LVDS Channel A Data3+	DP-0	-	-
A79	LVDS_A3-	LVDS_A_DATA3_N ; LVDS Channel A Data3-	DP-0	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CLK+	LVDS_A_CLK_P ; LVDS Channel A Clock+	DP-0	-	-
A82	LVDS_A_CLK-	LVDS_A_CLK_N ; LVDS Channel A Clock-	DP-0	-	-
A83	LVDS_I2C_CLK	LVDS_DDC_CLK ; JILI I2C Clock	I/O-3,3	PU 2k21 3,3V (s0)	-
A84	LVDS_I2C_DAT	LVDS_DDC_DATA ; JILI I2C Data	I/O-3,3	PU 2k21 3,3V (s0)	-
A85	GPI3	EXT_GPI3 ; General Purpose Input 3	I-3,3	PU 10k 3,3V (S0)	-

A86	KBD_RST#	KBD_RST# ; Keyboard Reset	I-3,3	PU 10k 3,3V (S0)	-
A87	KBD_A20GATE	KBD_A20GATE	I-3,3	PU 10k 3,3V (S0)	-
A88	PCIE0_CK_REF+	CLK_PCIE_CON_P	DP-0	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_CON_N	DP-0	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	Nc	-	-
A92	RSVD	n.c.	Nc	-	-
A93	GPO0	EXT_GPO0 ; General Purpose Output 0	O-3,3	PD 10k	-
A94	RSVD	n.c.	Nc	-	-
A95	RSVD	n.c.	Nc	-	-
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR	-	8.5-18V
A98	VCC_12V	12V VCC	PWR	-	8.5-18V
A99	VCC_12V	12V VCC	PWR	-	8.5-18V
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR	-	8.5-18V
A102	VCC_12V	12V VCC	PWR	-	8.5-18V
A103	VCC_12V	12V VCC	PWR	-	8.5-18V
A104	VCC_12V	12V VCC	PWR	-	8.5-18V
A105	VCC_12V	12V VCC	PWR	-	8.5-18V
A106	VCC_12V	12V VCC	PWR	-	8.5-18V
A107	VCC_12V	12V VCC	PWR	-	8.5-18V
A108	VCC_12V	12V VCC	PWR	-	8.5-18V
A109	VCC_12V	12V VCC	PWR	-	8.5-18V
A110	GND	Power Ground	PWR	-	-

4.2.3 Connector X1A Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	GBE0_ACT# ; Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC_FRAME# ; LPC Frame Indicator	I-3,3	-	-
B4	LPC_ADO	LPC_ADO ; LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B5	LPC_AD1	LPC_AD1 ; LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B6	LPC_AD2	LPC_AD2 ; LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B7	LPC_AD3	LPC_AD3 ; LPC Adress & DATA Bus	I/O-3,3	-	int. PU 20k in ICH9
B8	LPC_DRQ0#	LPC_DRQ#0 ; LPC Request 0	I-3,3	PU 10k 3,3V (S0)	int. PU 20k in ICH9
B9	LPC_DRQ1#	LPC_DRQ#1 ; LPC Request 1	I-3,3	PU 10k 3,3V (S0)	int. PU 20k in ICH10
B10	LPC_CLK	CLK_LPC_33M_EXT ; 33MHz LPC clock	O-3,3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	EXT_PWRBTN# ; Power Button	I-3,3	PU 20k 3,3V (S5)	-
B13	SMB_CLK	SMB_CLK_EXT ; SMBUS Clock	O-3,3	PU 2k2 3,3V (S5)	-
B14	SMB_DAT	SMB_DATA_EXT ; SMBUS Data	IO-3,3	PU 2k2 3,3V (S5)	-
B15	SMB_ALERT#	SMB_ALERT# ; SMBUS Interrupt	IO-3,3	PU 1k0 3,3V (S5)	-
B16	SATA1_TX+	SATA_TX1_P ; SATA 1 Transmit Data +	DP-0	-	-
B17	SATA1_TX-	SATA_TX1_N ; SATA 1 Transmit Data -	DP-0	-	-
B18	SUS_STAT#	PM_SUS_STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA_RX1_P ; SATA 1 Receive Data +	DP-I	-	-
B20	SATA1_RX-	SATA_RX1_N ; SATA 1 Receive Data -	DP-I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	SATA_TX3_P ; SATA 3 Transmit Data +	DP-0	-	-
B23	SATA3_TX-	SATA_TX3_N ; SATA 3 Transmit Data -	DP-0	-	-
B24	PWR_OK	EXT_PWR_OK ; Power OK	I-3,3	-	-
B25	SATA3_RX+	SATA_RX3_P ; SATA 3 Receive Data +	DP-I	-	-
B26	SATA3_RX-	SATA_RX3_N ; SATA 3 Receive Data -	DP-I	-	-
B27	WDT	WDT ; Watch Dog Timer	O-3,3	-	-
B28	AC_SDIN2	HDA_SDIN2_ICH ; HD Audio Serial Input Data 2	I-3,3	-	int. PD 20k in ICH9

B29	AC_SDIN1	HDA_SDIN1_ICH ; HD Audio Serial Input Data 1	I-3,3	-	int. PD 20k in ICH9
B30	AC_SDINO	HDA_SDINO_ICH ; HD Audio Serial Input Data 0	I-3,3	-	int. PD 20k in ICH9
B31	GND	Power Ground	PWR	-	-
B32	SPKR	HDA_SPKR ; Speaker	0-3,3	-	int. PD 20k in ICH9
B33	I2C_CLK	I2C_CLK_EXT ; I2C clock	0-3,3	PU 2k21 3,3V (S0)	-
B34	I2C_DAT	I2C_DATA_EXT ; I2C data	I/0-3,3	PU 2k21 3,3V (S0)	-
B35	THRM#	PM_THRM# ; Over Temperature	0-3,3	PU 8k25 3,3V (S0)	-
B36	USB7-	USB7_N ; USB Data - Port7	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B37	USB7+	USB7_P ; USB Data + Port7	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B38	USB_4_5_OC#	USB_45_OC# ; USB OverCurrent Port 4/5	I-3,3	PU 10k 3,3V (S5)	-
B39	USB5-	USB5_N ; USB Data - Port5	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B40	USB5+	USB5_P ; USB Data + Port5	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB3_N ; USB Data - Port3	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B43	USB3+	USB3_P ; USB Data + Port3	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B44	USB_0_1_OC#	USB_01_OC# ; USB OverCurrent Port 0/1	I-3,3	PU 10k 3,3V (S5)	-
B45	USB1-	USB1_N ; USB Data - Port1	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B46	USB1+	USB1_P ; USB Data + Port1	DP-I/0	-	int. PD 15k in ICH9 ; 5V tolerant
B47	EXCD1_PERST#	EXCD1_PERST# ; Express card reset	0-3,3	-	-
B48	EXCD1_CPPE#	EXCD1_CPPE# ; capable c. request	I-3,3	PU 10k 3,3V (S5)	-
B49	SYS_RESET#	EXT_SYS_RESET# ; Reset Input	I-3,3	PU 10k 3,3V (S5)	-
B50	CB_RESET#	CB_RESET# ; Carrier board Reset	0-3,3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	opt. PCI Express lane 5 + Recieve	Nc	-	just available if no GbEthernet PHY is used.
B53	PCIE_RX5-	opt. PCI Express lane 5 - Recieve	Nc	-	just available if no GbEthernet PHY is used.
B54	GPO1	EXT_GPO1 ; General Purpose Output 1	0-3,3	PD 10k	-
B55	PCIE_RX4+	PCI Express lane 4 + Recieve	DP-I	-	available when ICH9-MDH or -R
B56	PCIE_RX4-	PCI Express lane 4 - Recieve	DP-I	-	available when ICH9-MDH or -R

B57	GPO2	EXT_GPO2 ; General Purpose Output 2	0-3,3	PD 10k	-
B58	PCIE_RX3+	PCI Express lane 3 + Recieve	DP-I	-	available when ICH9-MDH or -R
B59	PCIE_RX3-	PCI Express lane 3 - Recieve	DP-I	-	available when ICH9-MDH or -R
B60	GND	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCI Express lane 2 + Recieve	DP-I	-	-
B62	PCIE_RX2-	PCI Express lane 2 - Recieve	DP-I	-	-
B63	GPO3	EXT_GPO3 ; General Purpose Output 3	0-3,3	PD 10k	-
B64	PCIE_RX1+	PCI Express lane 1 + Recieve	DP-I	-	-
B65	PCIE_RX1-	PCI Express lane 1 - Recieve	DP-I	-	-
B66	WAKE0#	PCIE_WAKE#	IO-3,3	PU 1k0 3,3V (S5)	-
B67	WAKE1#	WAKE1#	I-3,3	PU 10k 3,3V (S5)	-
B68	PCIE_RX0+	PCI Express lane 0 + Recieve	DP-I	-	-
B69	PCIE_RX0-	PCI Express lane 0 - Recieve	DP-I	-	-
B70	GND	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS_B_DATA0_P ; LVDS Channel B Data0+	DP-0	-	-
B72	LVDS_B0-	LVDS_B_DATA0_N ; LVDS Channel B Data0-	DP-0	-	-
B73	LVDS_B1+	LVDS_B_DATA1_P ; LVDS Channel B Data1+	DP-0	-	-
B74	LVDS_B1-	LVDS_B_DATA1_N ; LVDS Channel B Data1-	DP-0	-	-
B75	LVDS_B2+	LVDS_B_DATA2_P ; LVDS Channel B Data2+	DP-0	-	-
B76	LVDS_B2-	LVDS_B_DATA2_N ; LVDS Channel B Data2-	DP-0	-	-
B77	LVDS_B3+	LVDS_B_DATA3_P ; LVDS Channel B Data3+	DP-0	-	-
B78	LVDS_B3-	LVDS_B_DATA3_N ; LVDS Channel B Data3-	DP-0	-	-
B79	LVDS_BKLT_EN	LVDS_BKLT_CTRL ; Panel Backlight ON	0-3,3	PD 100k	-
B80	GND	Power Ground	PWR	-	-
B81	LVDS_B_CLK+	LVDS_B_CLK_P ; LVDS Channel B Clock+	DP-0	-	-
B82	LVDS_B_CLK-	LVDS_B_CLK_N ; LVDS Channel B Clock-	DP-0	-	-
B83	LVDS_BKLT_CTRL	LVDS_BKLT_CTRL ; Backlight Brightness Contr.	0-3,3	-	-
B84	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B85	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B86	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-

B87	VCC_5V_SBY	+V_STBY_ETX ; 5V Standby	PWR 5V (S5)	-	-
B88	RSVD	n.c.	nc	-	-
B89	VGA_RED	CRT_RED ; Analog Video RGB-RED	OA	PD 150R	-
B90	GND	Power Ground	PWR	-	-
B91	VGA_GRN	CRT_GREEN ; Analog Video RGB-GREEN	OA	PD 150R	-
B92	VGA_BLU	CRT_BLUE ; Analog Video RGB-BLUE	OA	PD 150R	-
B93	VGA_HSYNC	CRT_HSYNC ; Analog Video H-Sync	0-3,3	-	-
B94	VGA_VSYNC	CRT_VSYNC ; Analog Video V-Sync	0-3,3	-	-
B95	VGA_I2C_CLK	CRT_DDC_CLK ; Display Data Channel Clock	I/O-5	PU 2k21 5V (S0)	-
B96	VGA_I2C_DAT	CRT_DDC_DATA ; Display Data Channel Data	I/O-5	PU 2k21 5V (S0)	-
B97	TV_DAC_A	TV_DACA_CVBS ; Composite CVBS	OA	PD 150R	-
B98	TV_DAC_B	TV_DADB_Y ; TV Luminance Signal	OA	PD 150R	-
B99	TV_DAC_C	TV_DADC_C ; TV Chrominance Signal	OA	PD 150R	-
B100	GND	Power Ground	PWR	-	-
B101	VCC_12V	12V VCC	PWR	-	8.5-18V
B102	VCC_12V	12V VCC	PWR	-	8.5-18V
B103	VCC_12V	12V VCC	PWR	-	8.5-18V
B104	VCC_12V	12V VCC	PWR	-	8.5-18V
B105	VCC_12V	12V VCC	PWR	-	8.5-18V
B106	VCC_12V	12V VCC	PWR	-	8.5-18V
B107	VCC_12V	12V VCC	PWR	-	8.5-18V
B108	VCC_12V	12V VCC	PWR	-	8.5-18V
B109	VCC_12V	12V VCC	PWR	-	8.5-18V
B110	GND	Power Ground	PWR	-	-

4.2.4 Connector X1B Row C

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	PD 10k	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-5T	PU 4k7 3,3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-3,3	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-3,3	-	int. PU 20k in ICH9
C16	PCI_GNT2#	PCI Bus Grant 2	0-3,3	-	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 3,3V (S0)	-
C18	PCI_GNT1#	PCI Bus Grant 1	0-3,3	-	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 3,3V (S0)	-
C20	PCI_GNT0#	PCI Bus Grant 0	0-3,3	PD 1k0	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Request 0	I-5T	PU 8k2 3,3V (S0)	-
C23	PCI_RST#	PCI Bus Reset	0-3,3	-	-
C24	PCI_AD0	PCI Address & Data Bus line	I/O-5T	-	-
C25	PCI_AD2	PCI Address & Data Bus line	I/O-5T	-	-
C26	PCI_AD4	PCI Address & Data Bus line	I/O-5T	-	-
C27	PCI_AD6	PCI Address & Data Bus line	I/O-5T	-	-
C28	PCI_AD8	PCI Address & Data Bus line	I/O-5T	-	-
C29	PCI_AD10	PCI Address & Data Bus line	I/O-5T	-	-
C30	PCI_AD12	PCI Address & Data Bus line	I/O-5T	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Address & Data Bus line	I/O-5T	-	-
C33	PCI_C/BE1#	PCI Bus Cmd Byte enables 1	I/O-5T	-	-
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 3,3V (S0)	-
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 3,3V (S0)	-
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 3,3V (S0)	-
C37	PCI_IRDY#	PCI Bus Initiator Ready	I/O-5T	PU 8k2 3,3V (S0)	-
C38	PCI_C/BE2#	PCI Bus Cmd Byte enables 2	I/O-5T	-	-
C39	PCI_AD17	PCI Address & Data Bus line	I/O-5T	-	-
C40	PCI_AD19	PCI Address & Data Bus line	I/O-5T	-	-
C41	GND	Power Ground	PWR	-	-

C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	-
C44	PCI_C/BE3#	PCI Bus Cmd Byte enables 3	I/O-5T	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 3,3V (S0)	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 3,3V (S0)	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIexpress Graphics Recieve + (0)	DP-I	-	-
C53	PEG_RX0-	PCIexpress Graphics Recieve - (0)	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	PCIexpress Graphics Recieve + (1)	DP-I	-	-
C56	PEG_RX1-	PCIexpress Graphics Recieve - (1)	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	PCIexpress Graphics Recieve + (2)	DP-I	-	-
C59	PEG_RX2-	PCIexpress Graphics Recieve - (2)	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIexpress Graphics Recieve + (3)	DP-I	-	-
C62	PEG_RX3-	PCIexpress Graphics Recieve - (3)	DP-I	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-
C65	PEG_RX4+	PCIexpress Graphics Recieve + (4)	DP-I	-	-
C66	PEG_RX4-	PCIexpress Graphics Recieve - (4)	DP-I	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	PCIexpress Graphics Recieve + (5)	DP-I	-	-
C69	PEG_RX5-	PCIexpress Graphics Recieve - (5)	DP-I	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIexpress Graphics Recieve + (6)	DP-I	-	-
C72	PEG_RX6-	PCIexpress Graphics Recieve - (6)	DP-I	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-3,3	-	opt. PU 2k21 3,3V (S0) = enable SDVO/HDMI/DP interface
C74	PEG_RX7+	PCIexpress Graphics Recieve + (7)	DP-I	-	-
C75	PEG_RX7-	PCIexpress Graphics Recieve -	DP-I	-	-

		(7)			
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	PCIexpress Graphics Recieve + (8)	DP-I	-	-
C79	PEG_RX8-	PCIexpress Graphics Recieve - (8)	DP-I	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIexpress Graphics Recieve + (9)	DP-I	-	-
C82	PEG_RX9-	PCIexpress Graphics Recieve - (9)	DP-I	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIexpress Graphics Recieve + (10)	DP-I	-	-
C86	PEG_RX10-	PCIexpress Graphics Recieve - (10)	DP-I	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIexpress Graphics Recieve + (11)	DP-I	-	-
C89	PEG_RX11-	PCIexpress Graphics Recieve - (11)	DP-I	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIexpress Graphics Recieve + (12)	DP-I	-	-
C92	PEG_RX12-	PCIexpress Graphics Recieve - (12)	DP-I	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIexpress Graphics Recieve + (13)	DP-I	-	-
C95	PEG_RX13-	PCIexpress Graphics Recieve - (13)	DP-I	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	PCIexpress Graphics Recieve + (14)	DP-I	-	-
C99	PEG_RX14-	PCIexpress Graphics Recieve - (14)	DP-I	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIexpress Graphics Recieve + (15)	DP-I	-	-
C102	PEG_RX15-	PCIexpress Graphics Recieve - (15)	DP-I	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	8.5-18V
C106	VCC_12V	12V VCC	PWR	-	8.5-18V
C105	VCC_12V	12V VCC	PWR	-	8.5-18V
C107	VCC_12V	12V VCC	PWR	-	8.5-18V
C108	VCC_12V	12V VCC	PWR	-	8.5-18V
C109	VCC_12V	12V VCC	PWR	-	8.5-18V

C110	GND	Power Ground	PWR	-	-
------	-----	--------------	-----	---	---

4.2.5 Connector X1B Row D

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	PD 5k62	-
D9	IDE_IOW#	IDE IO Write	0-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	0-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k	-
D13	IDE_A0	IDE Adress Bus	0-3,3	-	-
D14	IDE_A1	IDE Adress Bus	0-3,3	-	-
D15	IDE_A2	IDE Adress Bus	0-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	0-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	0-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	0-3,3	-	int. PU 31k in PATA bridge ; not 5V tolerant
D19	PCI_GNT3#	PCI Bus Grant 3	0-3,3	-	int. PU 20k in ICH9 (if PCIRST#=0 AND PWROK=1)
D20	PCI_REQ3#	PCI Bus Request 0	I-5T	PU 8k2 3,3V (S0)	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	-
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 3,3V (S0)	-
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 3,3V (S0)	-
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 3,3V (S0)	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 3,3V (S0)	-
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	-

D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 3,3V (S0)	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 3,3V (S0)	-
D48	PCI_CLKRUN#	PCI Clock Run	I-5T	PU 8k25 3,3V (S0)	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	CLK_PCI_33M_EXT ; PCI Clock 33MHz	0-3,3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIexpress Graphics Transmit + (0)	DP-0	-	-
D53	PEG_TX0-	PCIexpress Graphics Transmit - (0)	DP-0	-	-
D54	PEG_LANE_RV#	PCIexpress Graphics Lane Reversal	I-3,3	-	-
D55	PEG_TX1+	PCIexpress Graphics Transmit + (1)	DP-0	-	-
D56	PEG_TX1-	PCIexpress Graphics Transmit - (1)	DP-0	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	PCIexpress Graphics Transmit + (2)	DP-0	-	-
D59	PEG_TX2-	PCIexpress Graphics Transmit - (2)	DP-0	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	PCIexpress Graphics Transmit + (3)	DP-0	-	-
D62	PEG_TX3-	PCIexpress Graphics Transmit - (3)	DP-0	-	-
D63	RSVD	-	nc	-	-
D64	RSVD	-	nc	-	-
D65	PEG_TX4+	PCIexpress Graphics Transmit + (4)	DP-0	-	-
D66	PEG_TX4-	PCIexpress Graphics Transmit - (4)	DP-0	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIexpress Graphics Transmit + (5)	DP-0	-	-
D69	PEG_TX5-	PCIexpress Graphics Transmit - (5)	DP-0	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIexpress Graphics Transmit + (6)	DP-0	-	-
D72	PEG_TX6-	PCIexpress Graphics Transmit - (6)	DP-0	-	-
D73	SDVO_CLK	SDVO_CTRLCLK I	0-3,3	-	-
D74	PEG_TX7+	PCIexpress Graphics Transmit + (7)	DP-0	-	-
D75	PEG_TX7-	PCIexpress Graphics Transmit - (7)	DP-0	-	-
D76	GND	Power Ground	PWR	-	-

D77	IDE_CBLID	IDE_CBLID# ; IDE cable type detect	I/O-3,3	-	opt. int. PU in IDE flash
D78	PEG_TX8+	PCIexpress Graphics Transmit + (8)	DP-0	-	-
D79	PEG_TX8-	PCIexpress Graphics Transmit - (8)	DP-0	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIexpress Graphics Transmit + (9)	DP-0	-	-
D82	PEG_TX9-	PCIexpress Graphics Transmit - (9)	DP-0	-	-
D83	RSVD	n.c.	nc -	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIexpress Graphics Transmit + (10)	DP-0	-	-
D86	PEG_TX10-	PCIexpress Graphics Transmit - (10)	DP-0	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX1	1+ PCIexpress Graphics Transmit + (11)	DP-0	-	-
D89	PEG_TX11-	PCIexpress Graphics Transmit - (11)	DP-0	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	PCIexpress Graphics Transmit + (12)	DP-0	-	-
D92	PEG_TX12-	PCIexpress Graphics Transmit - (12)	DP-0	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIexpress Graphics Transmit + (13)	DP-0	-	-
D95	PEG_TX13-	PCIexpress Graphics Transmit - (13)	DP-0	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	PCIexpress Graphics Enable	I-3,3	PU 10k 3,3V (S0)	-
D98	PEG_TX14+	PCIexpress Graphics Transmit + (14)	DP-0	-	-
D99	PEG_TX14-	PCIexpress Graphics Transmit - (14)	DP-0	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIexpress Graphics Transmit + (15)	DP-0	-	-
D102	PEG_TX15-	PCIexpress Graphics Transmit - (15)	DP-0	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	8.5-18V
D105	VCC_12V	12V VCC	PWR	-	8.5-18V
D106	VCC_12V	12V VCC	PWR	-	8.5-18V
D107	VCC_12V	12V VCC	PWR	-	8.5-18V
D108	VCC_12V	12V VCC	PWR	-	8.5-18V
D109	VCC_12V	12V VCC	PWR	-	8.5-18V
D110	GND	Power Ground	PWR	-	-



The termination resistors in these tables are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.6 Alternative Pinout of HDMI

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	TMDS_B_CLK	HDMI Port B Clock
D62	PCIexpress Graphics Transmit - 3	TMDS_B_CLK#	HDMI port B Clock complement
D58	PCIexpress Graphics Transmit + 2	TMDS_B_DATA0	HDMI port B Data0
D59	PCIexpress Graphics Transmit - 2	TMDS_B_DATA0#	HDMI port B Data0 complement
D55	PCIexpress Graphics Transmit + 1	TMDS_B_DATA1	HDMI port B Data1
D56	PCIexpress Graphics Transmit - 1	TMDS_B_DATA1#	HDMI port B Data1 complement
D52	PCIexpress Graphics Transmit + 0	TMDS_B_DATA2	HDMI port B Data2
D53	PCIexpress Graphics Transmit - 0	TMDS_B_DATA2#	HDMI port B Data2 complement
C61	PCIexpress Graphics Receive + 3	TMDS_B_HPD#	HDMI port B Hot-plug detect
D74	PCIexpress Graphics Transmit + 7	TMDS_C_CLK	HDMI port C Clock
D75	PCIexpress Graphics Transmit - 7	TMDS_C_CLK#	HDMI port C Clock complement
D71	PCIexpress Graphics Transmit + 6	TMDS_C_DATA0	HDMI port C Data0
D72	PCIexpress Graphics Transmit - 6	TMDS_C_DATA0#	HDMI port C Data0 complement
D68	PCIexpress Graphics Transmit + 5	TMDS_C_DATA1	HDMI port C Data1
D69	PCIexpress Graphics Transmit - 5	TMDS_C_DATA1#	HDMI port C Data1 complement
D65	PCIexpress Graphics Transmit + 4	TMDS_C_DATA2	HDMI port C Data2
D66	PCIexpress Graphics Transmit - 4	TMDS_C_DATA2#	HDMI port C Data2 complement
C74	PCIexpress Graphics Receive + 7	TMDS_C_HDP#	HDMI port C Hot-plug detect

4.2.7 Alternative Pinout of Display Port

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	DPB_LANE3	Displayport B Lane3
D62	PCIexpress Graphics Transmit - 3	DPB_LANE3#	Displayport B Lane3 complement
D58	PCIexpress Graphics Transmit + 2	DPB_LANE2	Displayport B Lane2
D59	PCIexpress Graphics Transmit - 2	DPB_LANE2#	Displayport B Lane2 complement
D55	PCIexpress Graphics Transmit + 1	DPB_LANE1	Displayport B Lane1
D56	PCIexpress Graphics Transmit - 1	DPB_LANE1#	Displayport B Lane1 complement
D52	PCIexpress Graphics Transmit + 0	DPB_LANE0	Displayport B Lane0
D53	PCIexpress Graphics Transmit - 0	DPB_LANE0#	Displayport B Lane0 complement
C61	PCIexpress Graphics Receive + 3	DPB_HPD#	Displayport B Hot-plug detect
C58	PCIexpress Graphics Receive + 2	DPB_AUX	Displayport B Aux
C59	PCIexpress Graphics Receive - 2	DPB_AUX#	Displayport B Aux complement
D74	PCIexpress Graphics Transmit + 7	DPC_LANE3	Displayport C Lane3
D75	PCIexpress Graphics Transmit - 7	DPC_LANE3#	Displayport C Lane3 complement
D71	PCIexpress Graphics Transmit + 6	DPC_LANE2	Displayport C Lane2
D72	PCIexpress Graphics Transmit - 6	DPC_LANE2#	Displayport C Lane2 complement

D68	PCIexpress Graphics Transmit + 5	DPC_LANE1	Displayport C Lane1
D69	PCIexpress Graphics Transmit – 5	DPC_LANE1#	Displayport C Lane1 complement
D65	PCIexpress Graphics Transmit + 4	DPC_LANE0	Displayport C Lane0
D66	PCIexpress Graphics Transmit – 4	DPC_LANE0#	Displayport C Lane0 complement
C74	PCIexpress Graphics Receive + 7	DPC_HPDP#	Displayport C Hot-plug detect
C71	PCIexpress Graphics Receive + 6	DPC_AUX	Displayport C Aux
C72	PCIexpress Graphics Receive – 6	DPC_AUX#	Displayport C Aus complement
D88	PCIexpress Graphics Transmit + 11	DPD_LANE3	Displayport D Lane3
D89	PCIexpress Graphics Transmit – 11	DPD_LANE3#	Displayport D Lane3 complement
D85	PCIexpress Graphics Transmit + 10	DPD_LANE2	Displayport D Lane2
D86	PCIexpress Graphics Transmit – 10	DPD_LANE2#	Displayport D Lane2 complement
D81	PCIexpress Graphics Transmit + 9	DPD_LANE1	Displayport D Lane1
D82	PCIexpress Graphics Transmit – 9	DPD_LANE1#	Displayport D Lane1 complement
D78	PCIexpress Graphics Transmit + 8	DPD_LANE0	Displayport D Lane0
D77	PCIexpress Graphics Transmit – 8	DPD_LANE0#	Displayport D Lane0 complement
C88	PCIexpress Graphics Receive + 11	DPD_HPDP#	Displayport D Hot-plug detect
C85	PCIexpress Graphics Receive + 10	DPD_AUX	Displayport D Aux
C86	PCIexpress Graphics Receive – 10	DPD_AUX#	Displayport D Aus complement

4.3 Signal Description

4.3.1 PCIexpress x1 lanes

The PCI express x1 lanes is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the ETXexpress® / COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

The microETXexpress®-PC has 5 PCIe X1(6 PCIe X1 without LAN).

It is also possible to run the 1st 4 x1 lanes as 1 x4 lane. For that please pull-up the signal A33 and A29 to 3.3V on the baseboard.



Express Card hotplug functionality is only available, when in BIOS setup the PCIexpress lane is switched from [AUTO] which is default setting to [ENABLED]

4.3.2 USB

8 x USB 1.1/2.0 Host Ports are available on the microETXexpress®-PC.

USB Client Support: NO

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.3 SATA

The microETXexpress®-PC offers 3 x SATA 300 (SATA#0-2; SATA#3: Sata2Pata) ports to connect modern hard drive disks.

Following AHCI features are supported: NCQ, HotPlug, Staggered Spinup, eSATA, PortMultiplier

Following RAID Modes are supported:

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.4 Audio

The microETXexpress®-PC has an HD Audio interface.



Baseboards with AC'97 codec only are not supported.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

4.3.5 VGA Output

microETXexpress®-PC offers an analog VGA output to connect CRT and LCD monitors.

Configuration

The graphics controller requires the following resources:

- » An IRQ
- » Several I/O addresses
- » Memory-address blocks in high memory

The BIOS allocates the resources during graphic configuration. Many resources are set for compatibility with industry-standard settings.

4.3.6 LVDS Flat Panel Interface (JILI)

The interface for flat panels is the JUMPtect Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the ETXexpress® / COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.3.7 PCIexpress Graphics

The PCI express Graphics interface allows the connection of high performance graphics chips on a high bandwidth interface.

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.3.8 SDVO

The microETXexpress®-PC Serial Digital Video Output port has the following features:

- » Share its pins with the PEG interface
- » Serial Digital Video Out Port (DVOB & DVOC) support
- » Two 12-bit channels
- » The SDVO B/C ports can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the documentation for additional information.

4.3.9 HDMI

There is one HDMI port available shared together with PCIexpress Graphics, SDVO and Displayport.

4.3.10 Displayport

The Displayport is available shared together with PCIexpress Graphics, SDVO and Displayport

4.3.11 Ethernet

The Ethernet interface offers 10/100/1000 Mbit connections and is driven by the Intel® 82567 (Boazman). The device auto-negotiates the use of the different speed connections.

The ethernet interface operates at lowest power (<1W) when Gbit-Ethernet is fully active and supports functions as WOL (Wake On LAN), PXE (Preboot eXecution Environment) boot and Jumbo Frames.

For cable lengths and terminations on your baseboard please refer to the COM Express® Design Guide.

Configuration

The Ethernet controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

4.3.12 LPC

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus bridge, which is located in the . The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the COM Express® Design Guide maintained by PICMG. Please refer to the official PICMG documentation for additional information.

The LPC bus does not support DMA (Direct Memory Access).

This leads to limitations for ISA bus and SIO (standard I/O 's like Floppy or LPT interfaces) implementations. When more than one device is connected to the LPC bus a clock buffer is required!

4.3.13 Power Control

Power Good (PWR_OK)

The microETXexpress®-PC provides an external input for a power-good signal (Pin B24). The implementation of this subsystem complies with the COM Express™ Specification. PWR_OK is internally pulled up to 3.3V and must be high level to power on the module.

Power Button (PWRBTN#)

The power button (Pin B12) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50ms ($50\text{ms} \leq t < 4\text{s}$) at low level (Power Button Event).

Pressing the power button for at least 4seconds will turn off power to the module (Power Button Override).

Reset Button (SYS_RESET#)

The reset button (Pin B49) is available through the module connector described in the pinout list. The module will stay in reset as long as SYS_RESET# is grounded.

Power Supply

The microETXexpress®-PC has a wide range power input from 8.5V - 18V. The supply voltage is applied through the VCC pins (VCC) of the module connector.

4.3.14 Miscellaneous Circuits

Speaker

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the official PICMG documentation for additional information.

Battery

The implementation of this subsystem complies with the COM Express™ Specification. Implementation information is provided in the COM Express™ Design Guide. Refer to the official documentation maintained by PICMG for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

I2C Bus

For additional information, refer to the COM Express™ Design Guide, I2C application notes and JIDA specifications which are available at the [customer section](#) of Kontron's Website. See BIOS chapter for supported features and speed of I2C.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Intel® 82801IUX-SFF (ICH9M-SFF). The SMBus is a two wire bidirectional bus (clock and serial data) used for system management such as reading parameters from a memory card, and reading temperatures and voltages of system components. The SM Bus uses the same signaling scheme as an I2C bus.

5 Special Features

5.1 S5 Eco Mode

Kontron's new high-efficient power-off state S5 Eco enables lowest power-consumption in soft-off state – less than 1 mA compared to the regular S5 state this means a reduction by at least factor 200!

In the „normal“ S5 mode the board is supplied by 5V_Stb and needs usually up to 300mA just to stay off. This mode allows to be switched on by power button, RTC event and WakeOnLan, even when it is not necessary. The new S5 Eco mode reduces the current tremendously.

The S5 Eco Mode can be enabled in BIOS Setup, when the BIOS supports this feature.

Following prerequisites and consequences occur when S5 Eco Mode is enabled

- » The power button must be pressed at least for 200ms to switch on.
- » Wake via Powerbutton only.
- » „Power On After Power Fail“: only „stay off“ is possible

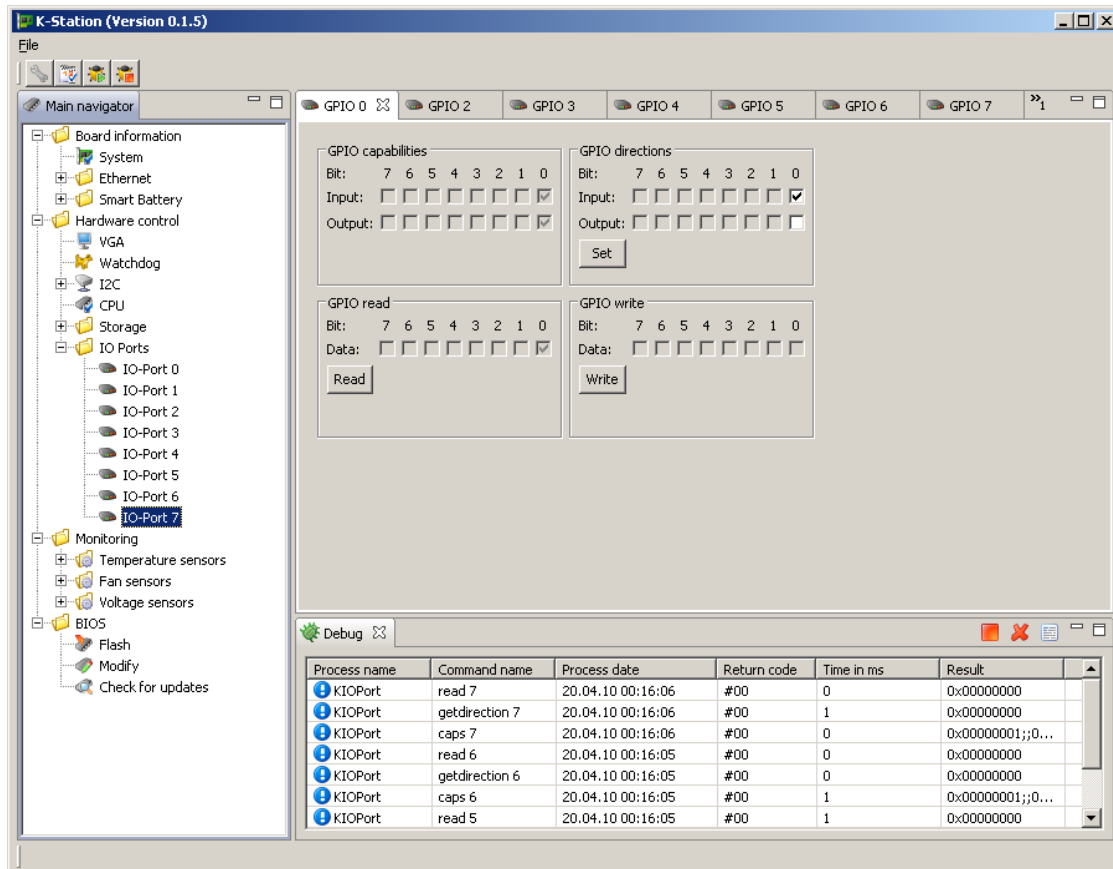
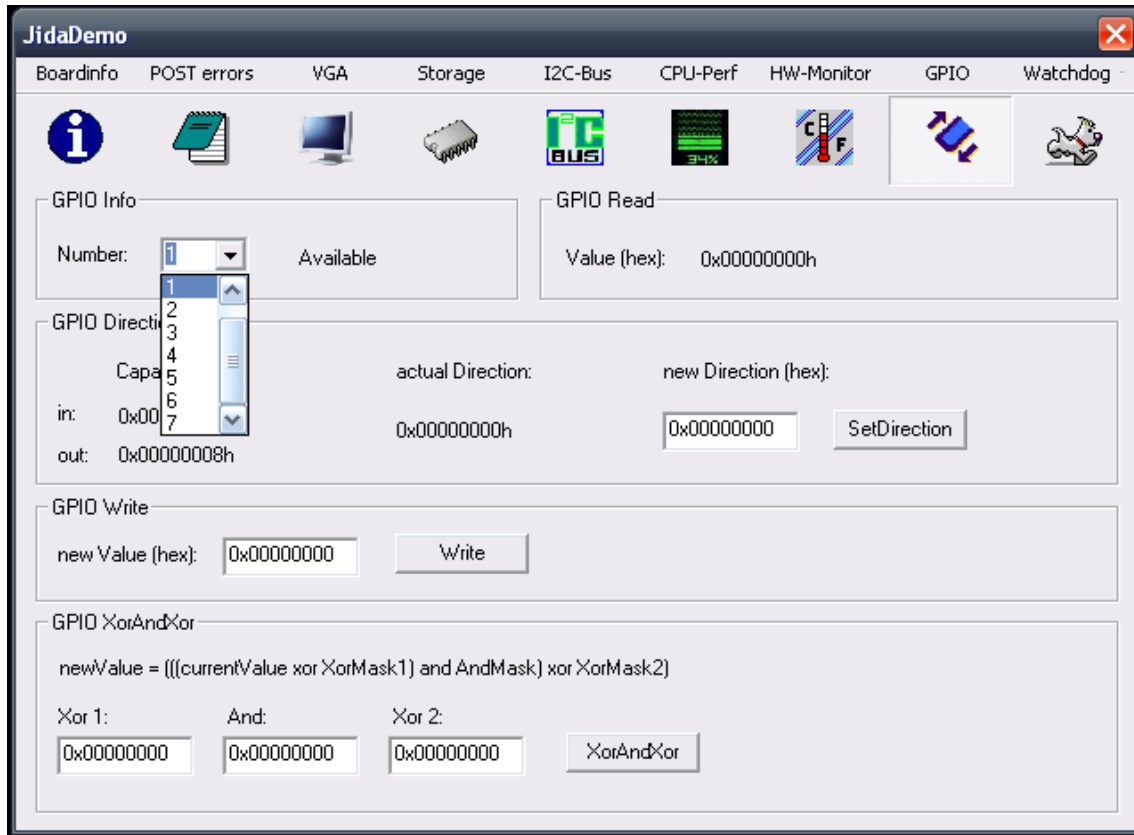
5.2 GPIO - General Purpose Input and Output

The microETXexpress®-PC offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

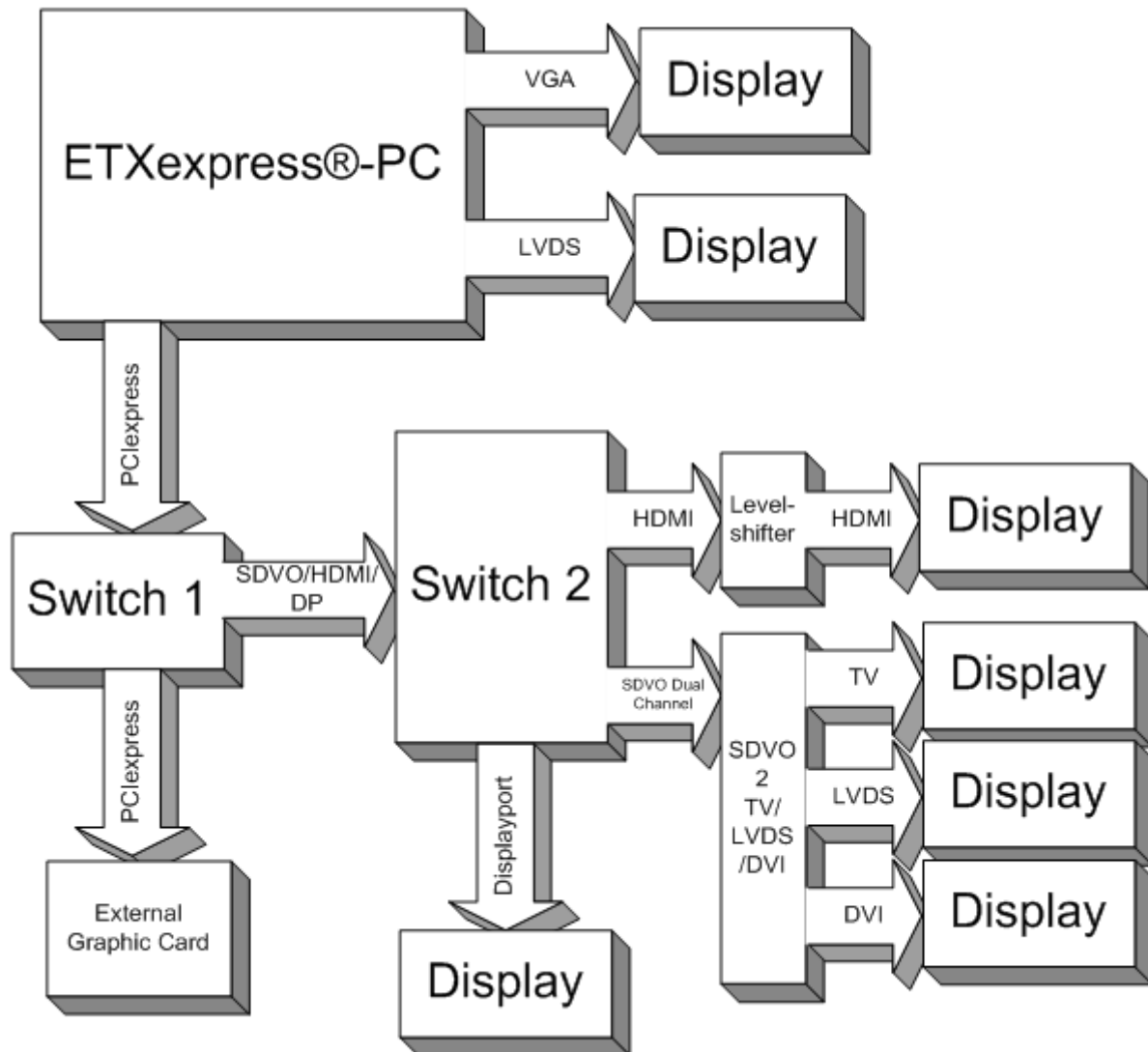
The GPI and GPO pins can be configured via JIDA32/K-Station. Please refer to the JIDA32/K-Station manual in the driver download packet on our [customer section](#).



5.3 Usage of Different Graphic Interfaces

The microETXexpress®-PC offers VGA, PCIexpress Graphics, LVDS, HDMI, SDVO and Displayport interfaces to connect graphical user interfaces. The usage of VGA, PCIexpress and SDVO complies with the current COM Express™ Specification.

The principle of using them is shown in the next drawing.



VGA and LVDS interface is always available and can be used. The pins of PCIexpress Graphics either are used as PCIexpress Graphics or as HDMI/SDVO/DP, which is controlled by switch1.

Switch1 is the SDVO_SDA# line (C73). When this signal is high (2.5V) the SDVO/HDMI/DP output is enabled. Otherwise the lines can be used as PCIexpressGraphic.

The switch 2 to select HDMI, SDVO or Displayport consists of the devices detected on the regarding sense circuits. When there is an SDVO 2 TV/LVDS/DVI converter found on the SDVO_DATA and _CLK lines (C73; D73) then the output is switched to SDVO. When there is Displayport device found on the Displayport AUX lines (C71; C72) then it is Displayport and in any other case the output is switched to HDMI.

5.4 Speedstep Technology

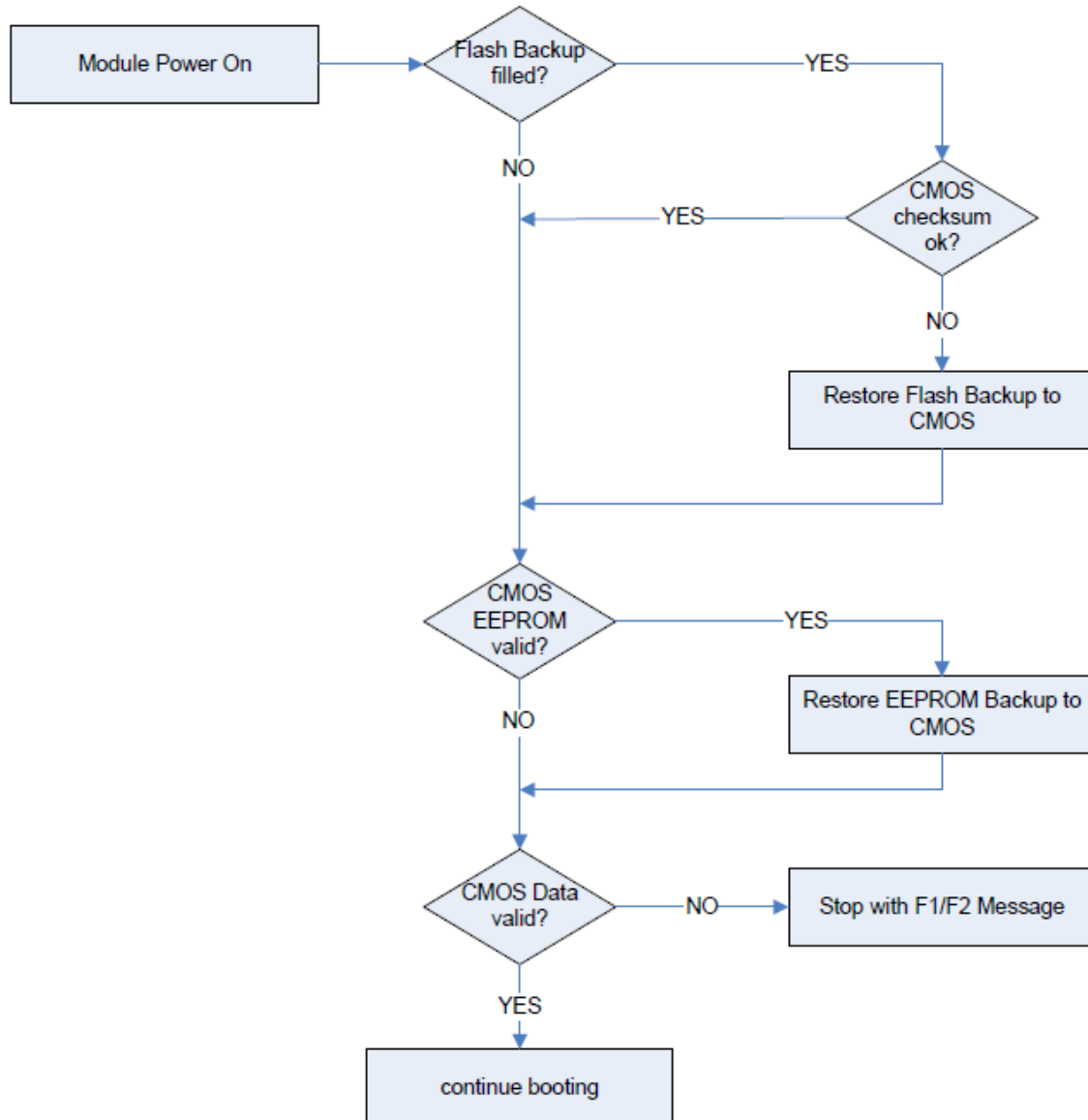
The Intel® processors offers the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It let you customize high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

By disabling the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

5.5 Flash Backup Feature

The microETXexpress®-PC supports a new functionality called "Flash Backup". This new feature allows saving custom defaults directly into the Flash. With invalid EEPROM data or without a CMOS EEPROM, the module will start up with these custom defaults. It's possible to save this BIOS with changed defaults to an image and flash it on other modules.



To create a BIOS with custom defaults:

- » Change your BIOS settings
- » Save as custom defaults to RTC/Flash and Exit (module will now always start with these settings)
- » Extract the BIOS including custom defaults with afudos or kflash utility for windows

Tool	Command
AFUDOS	<code>c:\>afudos.exe biosname.rom /O</code>
KFLASH	<code>c:\>kflash.exe backup biosname.rom</code>

Flash your BIOS with custom defaults: To flash a BIOS with customized defaults extracted like described above, use following options

Operating System	Command
Windows OS	<code>c:\>kflash.exe flash biosname.rom /bncr</code>
DOS	<code>c:\>afudos.exe biosname.rom /p /b /n /c</code> <code>c:\>jidacmos.exe eep /clean</code>



kflash.exe is a shell tool included in Kontron K-Station System Utility Package.
jidacmos utility is included in the BIOS download packages at Kontron's customer section.

5.6 Dynamic FSB Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency in half to further decrease the minimum processor operating frequency from the Enhanced Intel SpeedStep Technology performance states and achieve the Super Low Frequency Mode (Super LFM). This feature is supported at FSB frequencies of 1066 MHz, 800 MHz and 667 MHz and does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and GMCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. Both the processor and GMCH maintain a virtual BCLK signal (VBCLK) that is aligned to the external BCLK but at half the frequency.

After a downward shift, it would appear externally as if the bus is running with a 133-MHz base clock in all aspects, except that the actual external BCLK remains at 266 MHz. See Figure 3 for details. The transition into Super LFM, a “down-shift,” is done following a handshake between the processor and GMCH. A similar handshake is used to indicate an “up-shift,” a change back to normal operating mode. Please ensure this feature is enabled and supported in the BIOS.

5.7 Enhanced Intel Dynamic Acceleration Technology

The processor supports Intel Dynamic Acceleration Technology mode. The Intel Dynamic Acceleration Technology feature allows one core of the processor to operate at a higher frequency point when the other core is inactive and the operating system requests increased performance. This higher frequency is called the opportunistic frequency and the maximum rated operating frequency is the ensured frequency. The processor includes a hysteresis mechanism that improves overall Intel Dynamic Acceleration Technology performance by decreasing unnecessary transitions of the cores in and out of Intel Dynamic Acceleration Technology mode. Normally, the processor would exit Intel Dynamic Acceleration Technology as soon as two cores are active. This can become an issue if the idle core is frequently awakened for a short periods (i.e., high timer tick rates). The hysteresis mechanism allows two cores to be active for a limited time before it transitions out of Intel Dynamic Acceleration Technology mode.

Intel Dynamic Acceleration Technology mode enabling requires:

- » Exposure, via BIOS, of the opportunistic frequency as the highest ACPI P state

- » Enhanced Multi-Threaded Thermal Management (EMTTM)
- » Intel Dynamic Acceleration Technology mode and EMTTM MSR configuration via BIOS

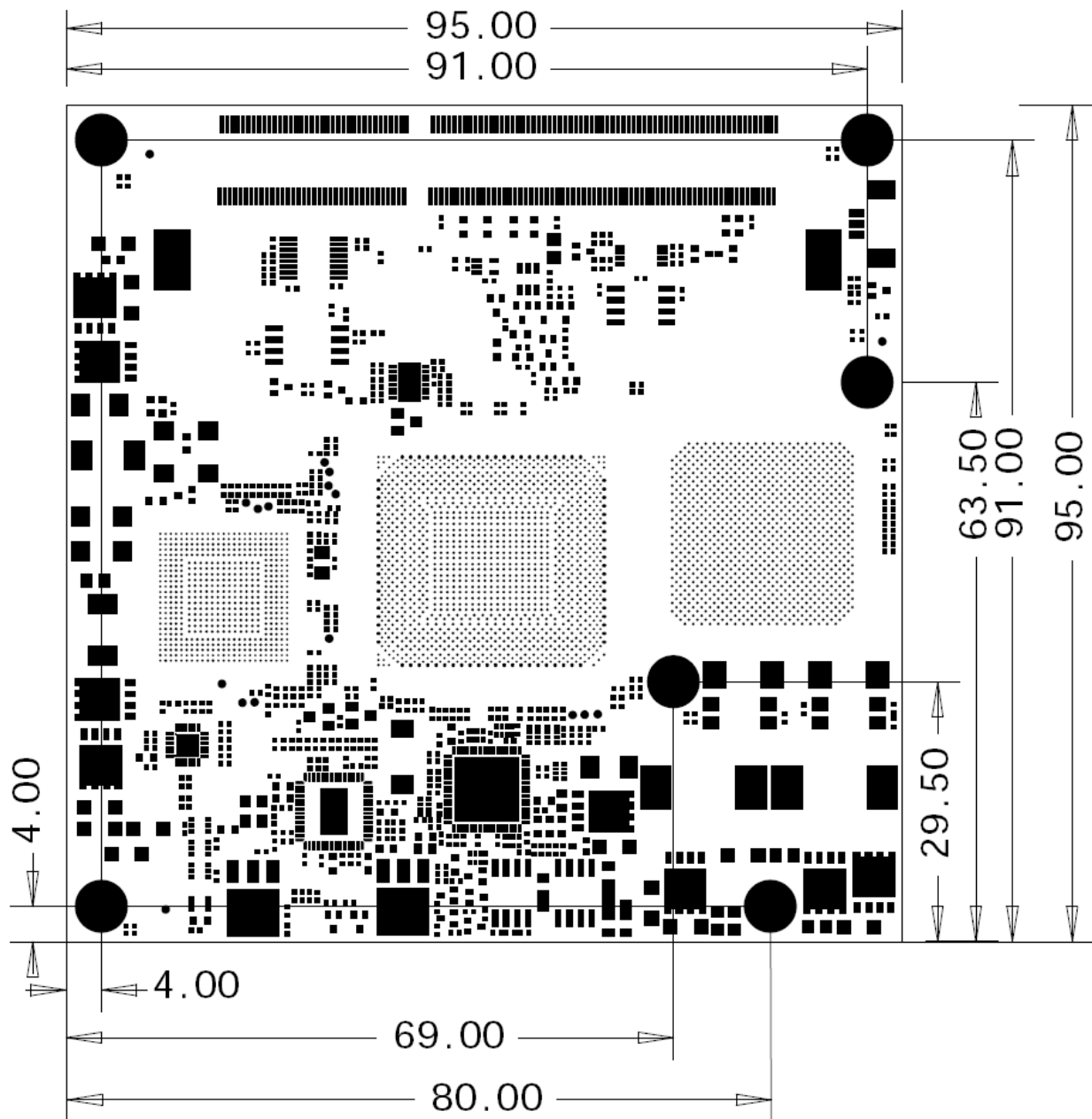
5.8 VID-x

The processor implements the VID-x feature for improved control of core voltage levels when the processor enters a reduced power consumption state. VID-x applies only when the processor is in the Intel Dynamic Acceleration Technology performance state and one or more cores are in low-power state (i.e., CC3/CC4/CC6). VID-x provides the ability for the processor to request core voltage level reductions greater than one VID tick. The amount of VID tick reduction is fixed and only occurs while the processor is in Intel Dynamic Acceleration Technology mode. This improved voltage regulator efficiency during periods of reduced power consumption allows for leakage current reduction which results in platform power savings and extended battery life.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw a Instantaneous current (ICC_CORE_INST) for a short duration of tINST; however, the average ICC current will be lesser than or equal to ICCDES current specification.

6 Design Consideration

6.1 Module Drillhole Dimension



6.2 Thermal Management

A heatspreader plate assembly is available from Kontron Embedded Modules for the microETXexpress®-PC. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express™-standard thermal interface to use with a heat sink or other cooling device.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heatspreader assembly implement thermal interfaces between the heatspreader plate and the major heat-generating components on the microETXexpress®-PC. About 80 percent of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution.

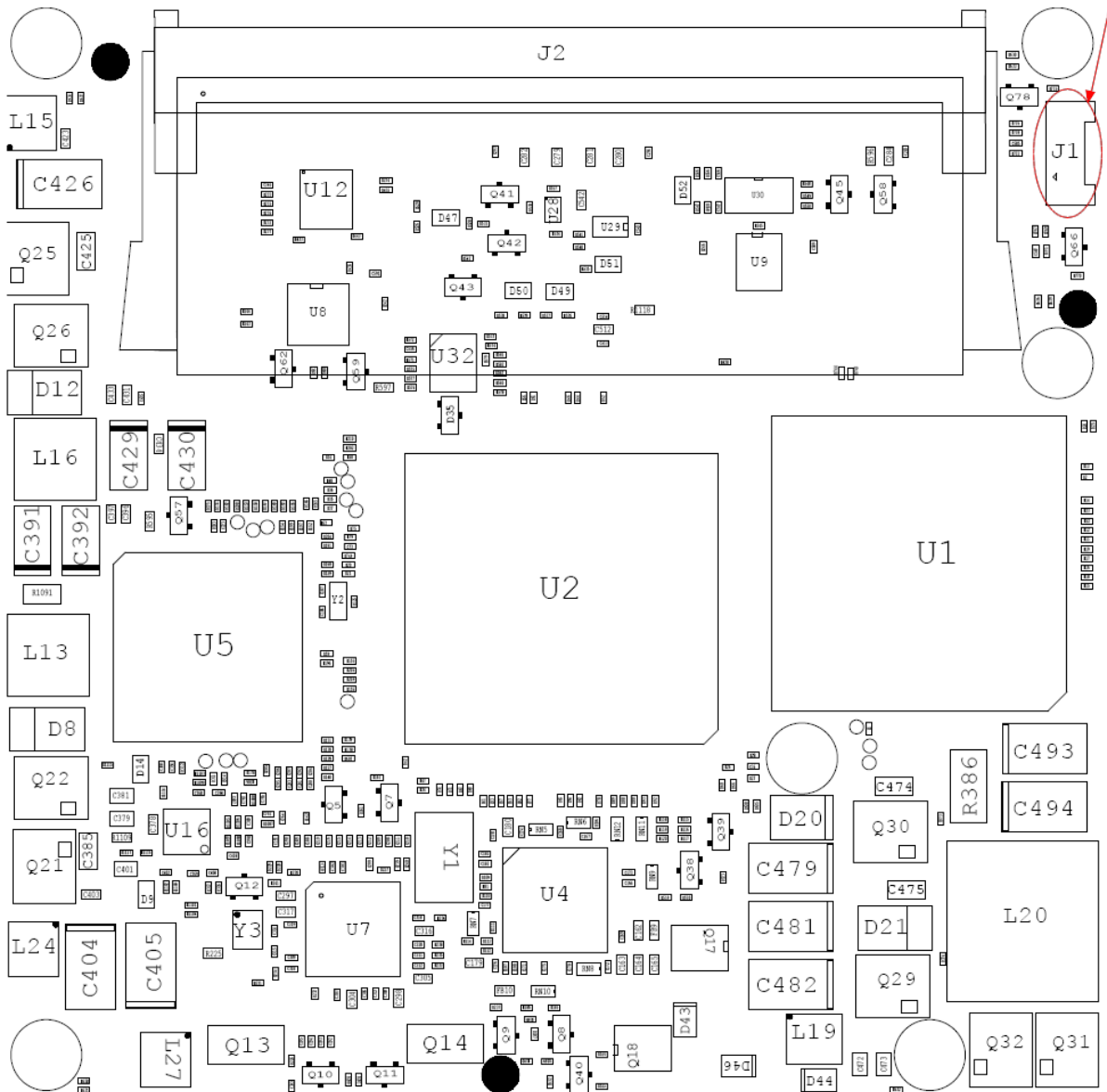
You can use many thermal-management solutions with the heatspreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express™ application and environmental conditions. Please see the COM Express™ Design Guide for further information on thermal management.

6.3 Heatspreader

Documentation of microETXexpress®-PC heatspreader and cooling solutions is provided at <http://emdcustomersection.kontron.com>.

6.4 Onboard Fan Connector

6.4.1 Location and Pinout of Fan Connector



The onboard fan connector (J1) can be found at the right side nearby the DRAM socket

Connector J1 has following specification:

- » Part number (Molex) J8: 53261-0390
- » Mates with: 51021-0300
- » Crimp terminals: 50079-8100

The Pin assignment is:

- » Pin1: Tacho
- » Pin2: VCC

» Pin3: GND

6.4.2 BIOS Settings for Fan Control

The fan can be controlled via the BIOS Settings „Advanced → Hardware Health → Module Hardware Health“



In general 4 modes are possible

- » Auto Fan Mode: Temperature Values can be selected to control the Fan
- » Fan Always On Full: Fan is always full on
- » Fan Disable Mode: Fan is disabled
- » Fan Manually Mode: A fixed PWM value (0...255) can be entered to run the fan at a selected speed

The used hardware monitor onboard is an ADT7475. For additional information please refer to the regarding datasheet.

6.4.3 Electrical Characteristics

There are 2 version of onboard fan control possible. Our standard modules have the simple version populated. For custom projects it is possible to populate a more sophisticated one. The differences are:

Features	Premium Fan	Base Fan
Input Voltage Range	8.5V - 18V	8.5V - 18V
Output Voltage	5V / 12V	Only 12V (switch in BIOS without function)
Max. output current	1A	0.3A



The fan voltage is in both versions VCC of the board and limited to 12V max.

The Fan out voltage output is not short circuit proof. If necessary the user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

With premium fan solution it is recommended to select the correct fan voltage first in BIOS setup and then connect the fan.

7 System Resources

7.1 Interrupt Request (IRQ) Lines

Please be aware that an ACPI OS decides itself on resource usage. The tables below show only an example distribution.

7.1.1 In 8259 PIC Mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	Note (4)
2	Slave 8259	No	
3		Yes	
4		Yes	
5		Yes	
6		Yes	
7		Yes	
8	RTC	No	
9	SCI	No	Note (3)
10		Yes	
11		Yes	
12	PS/2 Mouse	No	Note (5)
13	FPU	No	
14	IDE0	No	Note (1)(2)
15	IDE1	No	Note (1)(2)

1 If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

2 if sata controller is operating in legacy mode



3 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.

4 used by legacy keyboard controller when available on carrier board.

5 used by legacy ps/2 mouse controller when available on carrier board.

7.1.2 In APIC mode

IRQ#	Used For	Available	Comment
0	Timer 0	No	
1	Keyboard	No	
2	Slave 8259	No	
3		Yes	Note (4)
4		Yes	Note (4)
5		Yes	Note (4)
6		Yes	Note (4)
7		Yes	Note (4)
8	RTC	No	
9	SCI	No	Note (2)
10		Yes	Note (4)
11		Yes	Note (4)
12		Yes	Note (4)
13	FPU	No	
14	IDE0	No	Note (1)(3)
15	IDE1	No	Note (1)(3)
16	PIRQ[A]	For PCI	PCI IRQ line 1 + Graphics controller + HD Audio Controller + secondary IDE Note (4)
17	PIRQ[B]	For PCI	PCI IRQ line 2 + HD Audio controller Note (4)
18	PIRQ[C]	For PCI	PCI IRQ line 3 + USB UCHI controller #3 + SATA (native mode) Note (4)
19	PIRQ[D]	For PCI	PCI IRQ line 4 + USB UCHI controller #2 + IDE (native mode) Note (4)
20	PIRQ[E]	No	Lan Controller Note (4)
21	PIRQ[F]	No	Note (4)
22	PIRQ[G]	No	Note (4)
23	PIRQ[H]	No	USB EHCI controller, USB UCHI controller #1 Note (4)

1 If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.



2 Unavailable in Advanced Configuration and Power Interface (ACPI) mode. Used as System Control Interrupt (SCI) in ACPI mode. Currently not free in Non-ACPI mode.

3 IRQs are available if IDE controller is either disabled in setup or if in Native IDE mode.

4 ACPI Operating System decides on particular IRQ usage.

7.2 Direct Memory Access (DMA) Channels

DMA#	Used For	Available	Comment
0		No	
1		No	
2		No	
3		No	
4	Cascade	No	

5		No	
6		No	
7		No	

7.3 Memory Area

Upper Memory	Used For	Available	Comment
C0000h-CFFFFh	VGA BIOS	No	
D0000h-DFFFFh		Yes	LPC Bus or Shadow RAM
E0000h-EFFFFh	System BIOS	No	

7.4 I/O Address Map

Upper Memory	Used For	Available	Comment
400h-41Fh	Chipset	No	Always used by chipset
4D0h-4D1h	Interrupt Controller	No	
500h-53Fh	Chipset	No	Always used by chipset
800h-87Fh	Chipset	No	Always used by chipset
1000h>	PCI	No	

7.5 External Inter-IC (I2C) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
				2

7.6 System Management (SM) Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
10h	SMB Hoste	No	EEPROM for CMOS Data	1
12h	SMART_Charger	No	Only be used by a SMB Charger	1
14h	SMART_Selector	No	Only be used by a SMB Selector	1
16h	SMART_Battery	No	Only be used by a SMB Battery	1
2Eh	HW-Monitor	No		1
A0h	SPD	No		1
A2h	SPD	No		1
D2h	Clockgenerator	No		1

7.7 JILI I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	6
62h	MAX6253	No	DAC for Backlight brightness	6

7.8 SDVO I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	4

7.9 CRT I2C Bus

I2C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	DDC	No	Display Data	5

JIDA Bus Nr. 0 and Bus Nr. 3 are for internal use only.

7.10 K-Station / JIDA32 resources

7.10.1 I2C

BUS	Function
I2C 0	Internal / JIDA I2C
I2C 1	SM-Bus
I2C 2	external I2C
I2C 3	internal watchdog
I2C 4	SDVO DDC
I2C 5	CRT DDC
I2C 6	JILI DDC

7.10.2 Storage

Device	Function
EEPROM 0	JIDA EEPROM Area1 with 32 Bytes (free to use)

7.10.3 GPIO

Port	Function
IO-Port 0	GPI 0
IO-Port 1	GPI 1
IO-Port 2	GPI 2
IO-Port 3	GPI 3
IO-Port 4	GPO 0
IO-Port 5	GPO 1
IO-Port 6	GPO 2
IO-Port 7	GPO 3

7.10.4 Hardware Monitor

Sensor	Function
Temp 0	CPU temperature
Temp 1	internal HWM temperature (inside ADT7476)
Temp 2	chipset temperature (Intel® 4 series chipset)
Temp 3	external carrier board SIO Winbond 83627 Temp Sensor 0
Temp 3	external carrier board SIO Winbond 83627 Temp Sensor 1
Temp 5	external carrier board SIO Winbond 83627 Temp Sensor 2
FAN 0	CPU fan controlled by ADT7476
FAN 1	external carrier board SIO Winbond 83627 FAN Sensor 0

FAN 2	external carrier board SIO Winbond 83627 FAN Sensor 1
FAN 3	external carrier board SIO Winbond 83627 FAN Sensor 2
Voltage 0	internal ADT7476 battery voltage: VBAT
Voltage 1	external SIO Winbond 83627 CPU core voltage sensor: V CoreA
Voltage 2	external SIO Winbond 83627 battery voltage Sensor: VBAT
Voltage 3	external SIO Winbond 83627 Voltage Sensor 3: +3.3V
Voltage 4	external SIO Winbond 83627 Voltage Sensor 4: +5V
Voltage 5	external SIO Winbond 83627 standby Voltage Sensor 5: +5V sb

8 BIOS Operation

The module is equipped with AMI® BIOS, which is located in an onboard SPI serial flash memory. You can update the BIOS using a Flash utility.

8.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

- » AMIBIOS © 2006 American Megatrends, Inc.
- » BIOS Date: 05/11710 15:07:00 Ver: 08.00.15
- » Kontron® BIOS Version <UNTGRXXX
- » Copyright 2002-2010 Kontron Embedded Modules GmbH

8.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.



Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

8.2.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press when the following string appears during bootup.

Press to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▶) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

8.3 BIOS Setup

8.3.1 Main Menu

```

BIOS SETUP UTILITY
Main  Advanced  PCIPnP  Boot  Security  Chipset  Exit

System Overview
-----
Bios Info
Bios Version      : UNTGR410
AMI Core8 Version : 08.00.15
Build Date       : 04/20/10

▶ Module Info

System Time           [00:11:35]
System Date          [Tue 04/20/2010]

Displays Module Info

←  Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1  General Help
F10 Save and Exit
ESC  Exit

v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.

```

Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

8.3.2 Module Info

```

Module Info
Main

Module Info
Board Name      : Micro ETXexpress-PC
Board Class    : CPU
Serial Number   : UNTGBMD060006
Manufacturing Date : 5/5/2009
Hardware Revision : 3.2
Boot Counter   : 113

Processor
Intel(R) Core(TM)2 Duo CPU   L9400 @ 1.86GHz
Speed      : 1866MHz
Count     : 1

▶ Module Component Steppings
▶ Module Software Revisions
▶ Current LUDS Configuration
▶ Memory Module Information

Displays Module Component Steppings

←  Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1  General Help
F10 Save and Exit
ESC  Exit

v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.

```

Module Component Steppings

Module Component Steppings	
Main	
Module Component Steppings CPU Stepping : <0x010676> C0 NB Stepping : <0x07> B3 SB Stepping : <0x03> A3 WD PIC Revision : 1.3 KCPLD TYPE : N/A KCPLD REV : N/A	← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.	

Module Software Revisions

Module Software Revisions	
Main	
Module Software Revisions Bios Version : UNIGR410 Bios Build ID : 0.STABLE.219 CPU Microcode Rev : 12<0x0C> MRC Version : 02.91 GBE OPROM Version : 1.3.24 Intel Raid Version : 8.0.0.1038 JIDA32 Handler Revision : 1.3.53 Loader Revision : 1.1 JDA Revision : 1.11 UBIOS Revision : 1744 JILI Core Revision : 1.1.1 JRC Revision : 132	← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.	

Current LVDS Configuration

Main	
Current LVDS Configuration Data Source : Fixed Mode Resolution : 640x480 Color Depth : 18Bit Channel Count : Single Channel Dithering : Enabled	← Select Screen ↑↓ Select Item F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

Memory Module Information

System Memory	
Current Configuration FSB Frequency : 1066MHz Dual Channel Mode : Asymmetric DRAM Frequency : 1066 Mhz CAS# Latency (CL) : 7 RAS# to CAS# Delay (tRCD) : 7 RAS# Precharge (tRP) : 7 CycleTime (tRAS) : 20 System Memory Size :1949MB Memory Module Information ▶ SLOT 1	Displays Memory Module Information ← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.	

Slot 1

Main	
SLOT 1	
Technoligy	: DDR3 SDRAM
Manufacturer	: Qimonda
DRAM Manufacture	: Qimonda
Manufacture Loc	: 45
Manufacture Rev	: 1506
Partnum	: MSH1GS14A
S/N	: 10AC1749
Manufacture Date	: Week 35 /Year 08
Capacity	: 1024MB
Frequency	: DDR3-1066F, PC3-8500 533Mhz
SPD Revision	: 0.8
CRC	: UALID
	← Select Screen
	↑↓ Select Item
	F1 General Help
	F10 Save and Exit
	ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

8.3.3 Advanced Menu

BIOS SETUP UTILITY						
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
Advanced Settings						Configure CPU.
WARNING: Setting wrong values in below sections may cause system to malfunction.						
▶ CPU Configuration						
▶ IDE Configuration						
▶ AHCI Configuration						
▶ SuperIO Configuration						
▶ ACPI Configuration						
▶ PCI Express Configuration						
▶ USB Configuration						
▶ Hardware Health						
▶ Miscellaneous						
▶ Features						
						← Select Screen
						↑↓ Select Item
						Enter Go to Sub Screen
						F1 General Help
						F10 Save and Exit
						ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.						

CPU Configuration

BIOS SETUP UTILITY	
Advanced	
Configure advanced CPU settings Module Version:3F.11	
Manufacturer: Intel Intel(R) Core(TM)2 Duo CPU L9400 @ 1.86GHz Frequency :1.86GHz FSB Speed :1068MHz Cache L1 :64 KB Cache L2 :6144 KB Ratio Actual Value:7	
Hardware Prefetcher [Enabled] Adjacent Cache Line Prefetch [Enabled] Max CPUID Value Limit [Disabled] Intel(R) Virtualization Tech [Enabled] Execute-Disable Bit Capability [Enabled] DTS-based Thermal Management [Enabled] DTS Calibration [Enabled] Intel(R) SpeedStep(tm) tech [Enabled] Intel(R) C-STATE tech [Enabled] CPU Performance [High]	For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance to the specific application. ← Select Screen ↑↓ Select Item +− Change Option F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

Feature	Option	Description
Hardware Prefetcher	Enabled Disabled	For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance to the specific application.
Adjacent Cache Line Prefetch	Enabled Disabled	For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance to the specific application.
Max CPUID Value Limit	Disabled Enabled	Disabled for WindowsXP
Intel® Virtualization Tech	Enabled Disabled	When enabled, a VMM can utilize the additional HW Caps, provided by Intel® Virtualization Tech. Note: A full reset is required to change the setting.
Execute-Disable Bit Capability	Enabled Disabled	When disabled, force the XD feature flag to always return 0
DTS-based Thermal Management	Enabled Disabled	Enable/Disable Thermal Management utilizing the CPU's Digital Thermal Sensor
DTS Calibration	Enabled Disabled	Enables and Disables the Calibration function of the CPU's Digital Thermal Sensor
Intel® SpeedStep™	Enabled Disabled	Enables and Disables the SpeedStep power management feature
Intel® C-State Technology	Enabled Disabled	Enables and Disables the C - States. If enabled, the CPU is set to C2 - C4 state in idle mode
CPU Performance	High Middle Low	Select CPU Performance after POST

The CPU Performance relates to the used processor on the microETXexpress®-PC. The following table shows you the selected speed in the 3 performance stages.

Product Number	Processor	High	Middle	Low
36004-0000-19-2	SL9400	1,86GHz	1,6GHz	1,6GHz
36004-0000-12-2	SU9300	1,2GHz	1,2GHz	1,2GHz
36004-0000-12-1	CM722	1,2GHz	1,2GHz	1,2GHz
36004-0000-12-3	CM723	1,2GHz	1,2GHz	1,2GHz

IDE Configuration

BIOS SETUP UTILITY		
Advanced		
IDE Configuration		Options
SATA#1 Configuration	[Enabled]	Disabled
Configure SATA#1 as	[IDE Compatible]	Enabled
SATA#2 Configuration	[Enhanced]	
▶ Primary IDE Master	: [Not Detected]	
▶ Secondary IDE Master	: [Not Detected]	
▶ Third IDE Master	: [Not Detected]	
▶ Fourth IDE Master	: [Not Detected]	
Hard Disk Write Protect	[Disabled]	← Select Screen
IDE Detect Time Out (Sec)	[1]	↑↓ Select Item
ATA(PI) 80Pin Cable Detection	[Host & Device]	+− Change Option
		F1 General Help
		F10 Save and Exit
		ESC Exit
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.		

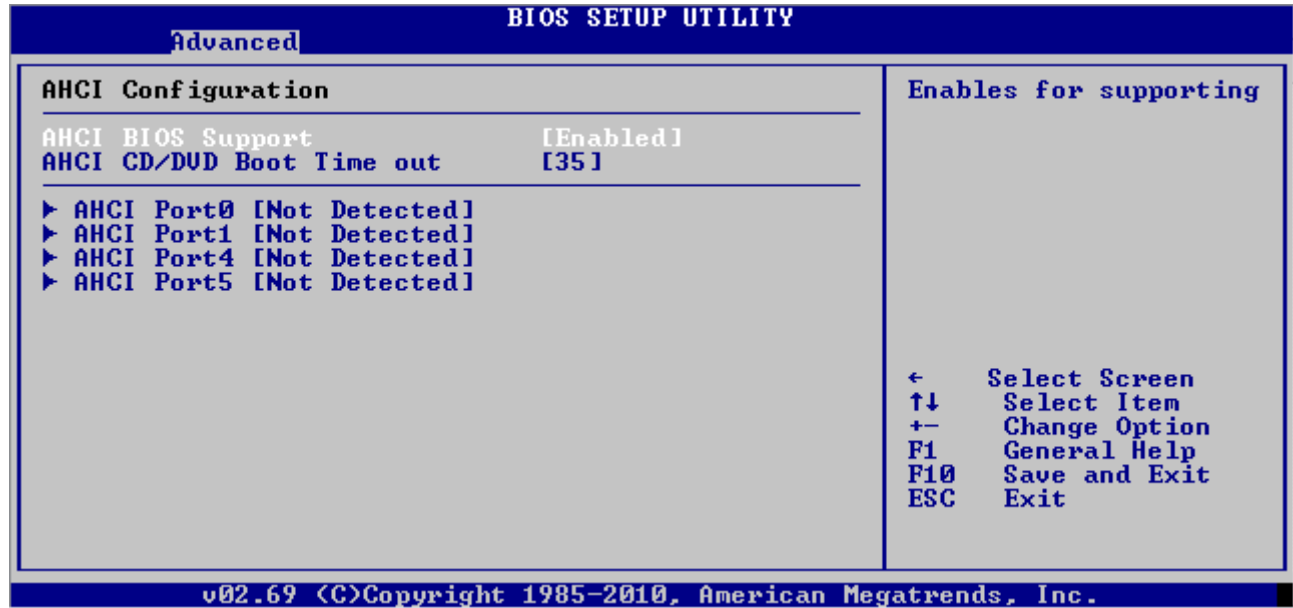
Feature	Option	Description
SATA #1 Configuration	Disabled Enabled	Enables or disables the IDE interface of US15W SCH. This concerns the onboard SSD and PATA2SATA Bridge
Configure SATA#1 as	IDE Compatible RAID AHCI IDE Enhanced	Selects the mode for SATA#1 controller
SATA#2 Configuration	Disabled Enhanced	Controls the mode for the 2nd SATA controller in ICH-9
Hard Disk Write Protect	Disabled Enabled	Disables/enables device write protection. It will be effective only if device is accessed through BIOS functions.
IDE Detect Time Out (Sec.)	[0-35] 1	Selects the time out value for the detection of ATA/ ATAPI devices
ATA(PI) 80Pin Cable Detection	Host & Device Host Device	Selects the mechanism for detecting 80Pin ATA(PI) cables.

IDE Device Submenu

Advanced		BIOS SETUP UTILITY	
Secondary IDE Master		Select the type of device connected to the system.	
Device	:Hard Disk		
Vendor	:WDC WD1600AAJS-56WAA0		
Size	:160.0GB		
LBA Mode	:Supported		
Block Mode	:16Sectors		
PIO Mode	:4		
Async DMA	:MultiWord DMA-2		
Ultra DMA	:Ultra DMA-6		
S.M.A.R.T.	:Supported		
Type	[Auto]	←	Select Screen
LBA/Large Mode	[Auto]	↑↓	Select Item
Block (Multi-Sector Transfer)	[Auto]	+−	Change Option
PIO Mode	[Auto]	F1	General Help
DMA Mode	[Auto]	F10	Save and Exit
S.M.A.R.T.	[Auto]	ESC	Exit
32Bit Data Transfer	[Disabled]		
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.			

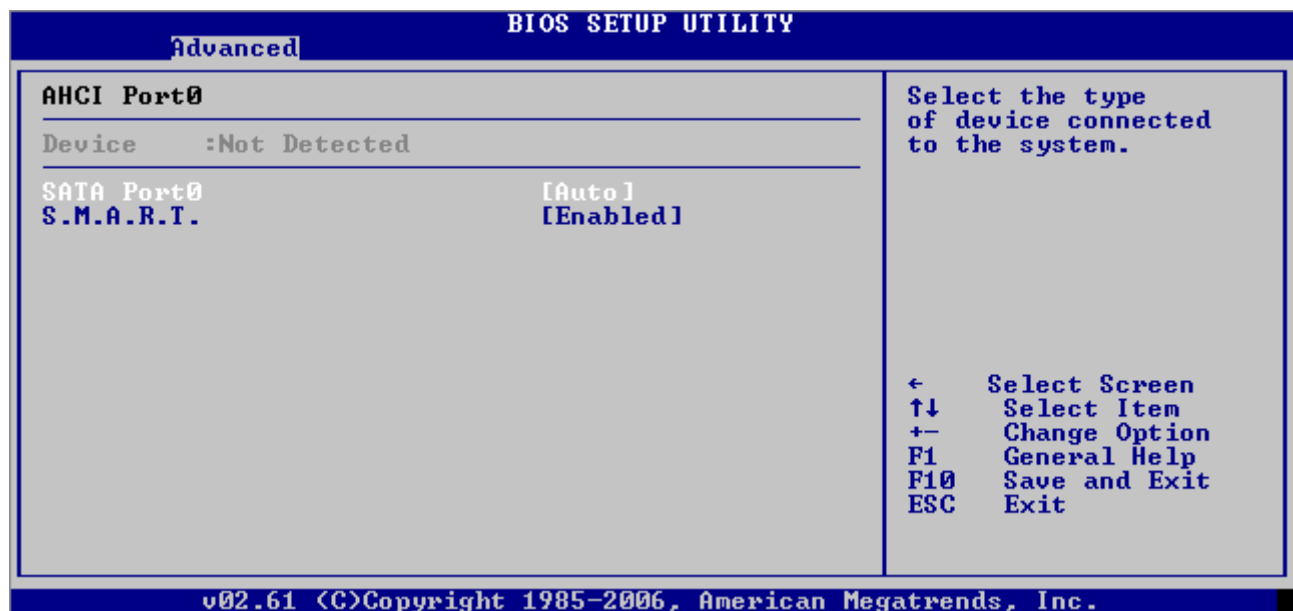
Feature	Option	Description
Type	Not Installed Auto CD/DVD ARMD	Selects the type of the IDE Devices connected to the system
LBA/Large Mode	Disabled Auto	Disables the LBA mode or enables it, when a device supports it
Block (Multi-Sector Transfer)	Disabled Auto	Disabled: The data transfer from and to the device occurs one sector at a time Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it
PIO Mode	Auto 0 1 2 3 4	(Auto) Configures the PIO Mode
DMA Mode	Auto SWDMA MWDMA UDMA	SWDMA: Single Word DMA MWDMA: Multi Word DMA UDMA: Ultra DMA
S.M.A.R.T.	Auto Enabled Disabled	Disables, Enables or automatically enables the S.M.A.R.T feature (Self-Monitoring, Analysis and Reporting Technology)
32Bit Data Transfer	Enabled Disabled	Disables and Enables the 32Bit Data Transfer Mode

AHCI Configuration



Feature	Option	Description
AHCI BIOS Support	Enabled Disabled	Enables / Disables the AHCI Support in BIOS
AHCI CD/DVD Boot Time out	0 5 10 ... 35	Selects the boot time out for AHCI CD/DVD devices

AHCI PortN Submenu



Feature	Option	Description
SATA Port 0	Auto Not installed	Enables / Disables this AHCI Port
S.M.A.R.T.	Disabled	Enables and disables the SMART functionality.

Enabled

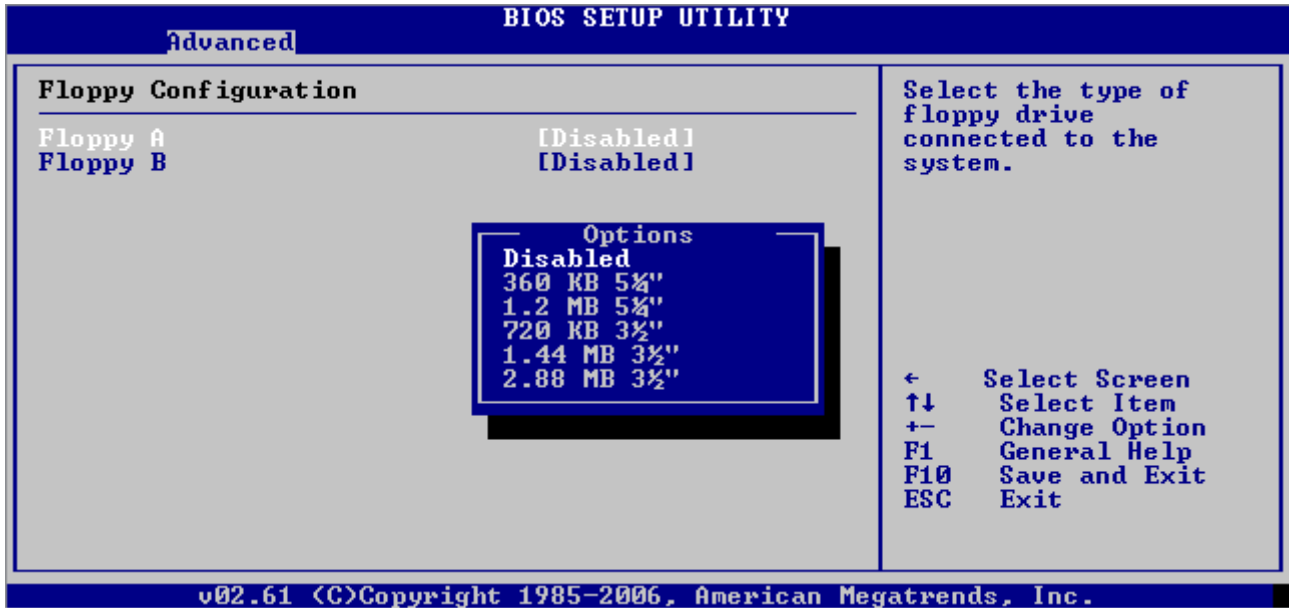
SuperIO Configuration

BIOS SETUP UTILITY	
Advanced	
Configure Win627 Super IO Chipset	
Floppy Controller	[Disabled]
Floppy Drive Swap	[Disabled]
▶ Floppy Configuration	
Serial Port1 Address	[3F8/IRQ4]
Serial Port2 Address	[Disabled]
Parallel Port Address	[378]
Parallel Port Mode	[SPP]
Parallel Port IRQ	[IRQ7]
Keyboard PowerOn	[Disabled]
Specific Key PowerOn	
Mouse PowerOn	[Disabled]
Allows BIOS to Enable or Disable Floppy Controller.	
← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit	
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.	

Feature	Option	Description
Floppy Controller	Disabled Enabled	Enables / Disables the AHCI Support in BIOS
Floppy Drive Swap	Disabled Enabled	If enabled floppy drive A and B are swapped.
Serial Port1 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 1
Serial Port2 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Selects the Address of COM Port 2
Parallel Port Address	Disabled 378 278 3BC	Selects the Address of the LPT Port
Parallel Port Mode	SPP Bi-Directional ECP EPP+SPP ECP+SPP	Allows BIOS to Select Parallel Port Mode
Parallel Port IRQ	IRQ5 IRQ7	Allows BIOS to Select Parallel Port IRQ
Keyboard Power On	Disabled Specific Key Any Key	Selects the Mode for PS/2 Keyboard Power On
Specific Key Power On	[Enter Key]	Only available when Specific Key is selected then „Enter New Password“

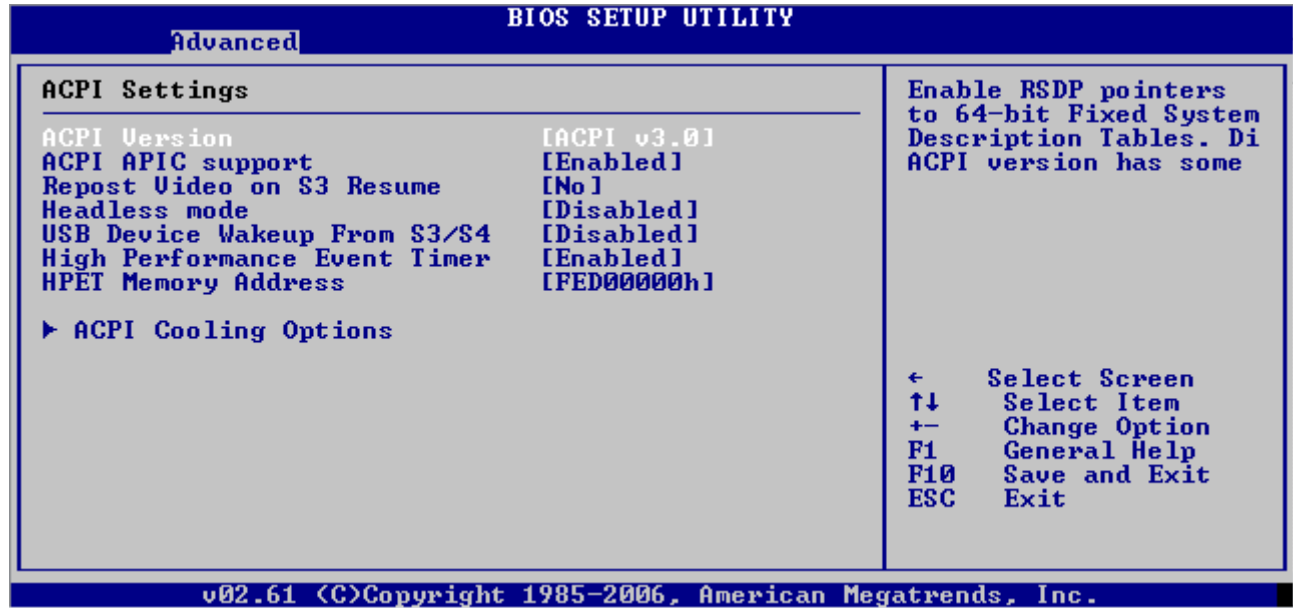
		Pop Up appears
Mouse Power On	Disables Left Button Right Button	Selects teh Mode for PS/2 Mouse Power On

Floppy Configuration Submenu



Feature	Option	Description
Floppy A	Disabled	Selects the Floppy Drive A
	360 KB 5 1/4"	
	1.2 MB 5 1/4"	
	720 KB 3 1/2"	
	1.44 MB 3 1/2"	
	2.88 MB 3 1/2"	
Floppy B	Disabled	Selects the Floppy Drive B
	360 KB 5 1/4"	
	1.2 MB 5 1/4"	
	720 KB 3 1/2"	
	1.44 MB 3 1/2"	
	2.88 MB 3 1/2"	

ACPI Configuration



Feature	Option	Description
ACPI Version	ACPI v.3.0 ACPI v.2.0 ACPI v.1.0	Selects the ACPI version
ACPI APIC support	Enabled Disabled	Include ACPI APIC table pointer to RSDT pointer list.
Repost Video on S3 Resume	No Yes	If yes, Videobios is reinitialized after S3 Resume
Headless Mode	Disabled Enabled	Enables / Disables headless mode through ACPI
USB Device Wakeup From S3/S4	Disabled Enabled	Enables / Disables the possibility to wake up via USB from S3 and S4
High Performance Event Timer	Disabled Enabled	Enables / Disables the High Performance Event Timer
HPET Memory Address	FED00000h FED01000h FED02000h FED03000h	Selects the Address of the High Performance Event Timer

ACPI Cooling Options

Advanced		BIOS SETUP UTILITY
ACPI Cooling Options		This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU. ← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
Passive Trip Point:	[80°C]	
Passive TC1 Value:	[1]	
Passive TC2 Value:	[5]	
Passive TSP Value:	[10]	
Critical Trip Point:	[110°C]	
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.		

Feature	Option	Description
Passive Trip Point	Disabled 40°C 45°C 50°C ... 110°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the CPU.
Passive TC1 value	1 2 3 ... 16	This value sets the TC1 value for the ACPI Passive Cooling Formula
Passive TC2 value	1 2 ... 5 ... 16	This value sets the TC2 value for the ACPI Passive Cooling Formula
Passive TSP value	2 4 ... 10 ... 30	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled
Critical Trip Point	Disabled 40°C 45°C 50°C ... 110°C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut off the system.

PCIExpress Configuration

BIOS SETUP UTILITY		
Advanced		
PCI Express Configuration		Enables/Disables Pci Express Device Relaxed Ordering.
Relaxed Ordering	[Auto]	
Maximum Payload Size	[Auto]	← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
Extended Tag Field	[Auto]	
No Snoop	[Auto]	
Maximum Read Request Size	[Auto]	
Active State Power Management	[Disabled]	
Extended Synch	[Auto]	
PCIE Port 0	[Auto]	
PCIE Port 1	[Auto]	
PCIE Port 2	[Auto]	
PCIE Port 3	[Auto]	
PCIE Port 4	[Auto]	
PCIE High Priority Port	[Disabled]	
PCIE Port 0 IOxAPIC Enable	[Disabled]	
PCIE Port 1 IOxAPIC Enable	[Disabled]	
PCIE Port 2 IOxAPIC Enable	[Disabled]	
PCIE Port 3 IOxAPIC Enable	[Disabled]	
PCIE Port 4 IOxAPIC Enable	[Disabled]	
PCIE Port 5 IOxAPIC Enable	[Disabled]	

v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.

Feature	Option	Description
Relaxed Ordering	Auto Disables Enabled	Enables/Disables PCI Express Device Relaxed Ordering.
Maximum Payload Size	Auto 128 Bytes ... 4096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
Extended Tag Field	Auto Disables Enabled	If Enabled, allows Device to use 8-bit TAG field as a requester.
No Snoop	Auto Disables Enabled	Enables/Disables PCI Express Device No Snoop option.
Maximum Read Request Size	Auto 128 Bytes ... 4096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.
Active State Power Management	Disabled Enabled	Enables/Disables PCI Express L0 and L1 link power states.
Extended Synch	Auto Disables Enabled	If Enabled, allows generation of Extended Synchronisation patterns.
PCIE Port N	Auto Enabled Disabled	Enables/Disables or autoconfigures the PCIE Port N
PCIE High Priority Port	Disabled Port 0 Port 1	Select the PCIE Port that gets higher priority than the others.

	Port 2 ... Port 5	
PCIE Port N IOxAPIC Enable	Disabled Enabled	Enables/Disables the APIC Support for the PCIE Port N

USB Configuration

BIOS SETUP UTILITY	
Advanced	
USB Configuration <hr/> Module Version - 2.24.5-13.4 USB Devices Enabled : 1 Keyboard, 1 Drive Legacy USB Support [Enabled] USB 2.0 Controller Mode [HiSpeed] BIOS EHCI Hand-Off [Enabled] Legacy USB1.1 HC Support [Enabled] USB Beep Message [Enabled] ▶ USB Mass Storage Device Configuration	Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected. ← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
v02.69 (C)Copyright 1985-2010, American Megatrends, Inc.	

Feature	Option	Description
Legacy USB Support	Auto Disabled Enabled	Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	Disabled Enabled	This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should claim by the EHCI driver
Legacy USB 1.1 HC Support	Disabled Enabled	Support USB 1.1 Host Controller
USB Beep Message	Disabled Enabled	Enables the beep during USB device enumeration

USB Mass Storage Device Configuration

Advanced		BIOS SETUP UTILITY	
USB Mass Storage Device Configuration USB Mass Storage Reset Delay [20 Sec] Device #1 Ut165 S ¹ Emulation Type [Auto]		Number of seconds POST waits for the USB mass storage device after start unit command. ← Select Screen ↑↓ Select Item +− Change Option F1 General Help F10 Save and Exit ESC Exit	
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.			

Feature	Option	Description
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	If Auto USB devices with less than 530MB will be emulated as floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

Hardware Health

Advanced		BIOS SETUP UTILITY	
Hardware Health Configuration ▶ Module Hardware Health Configuration ▶ BaseBoard Hardware Health Configuration		Configure/monitor the Hardware Health of the Module ← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit	
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.			

Module Hardware Health Configuration

Advanced		BIOS SETUP UTILITY	
Module Hardware Health Configuration		Enables Hardware Health Monitoring Device.	
H/W Health Function	[Enabled]	← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit	
PWM 1 Mode Setting	[Fan Manually Mode]		
PWM 1 Ramp Rate	[Time Slot 1]		
PWM 1 Control Duty Cycle	[200]		
Pulses/Rev	[2]		
Fan Voltage	[5V]		
CPU Temperature	:49°C/120°F		
Internal Temperature	:38°C/100°F		
Northbridge Temperature	:36°C/96°F		
Fan1 Speed	: N/A		
3.3 V supply voltage	: 3.29 V		
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.			

Feature	Option	Description
H/W Health Function	Disabled Enabled	Enables Hardware Health Monitoring Device.
PWM 1 Mode Setting	Auto Fan Mode Fan Always On Full Fan Disable Mode Fan Manually Mode	PWM Configuration Mode Setting
PWM 1 Ramp Rate	Time Slot 1 Time Slot 2 Time Slot 3 Time Slot 4 Time Slot 8 Time Slot 12 Time Slot 24 Time Slot 48	
PWM 1 Control Duty Cycle	[0...255]	Controls the length of a PWM duty cycle.
Pulses/Rev	[1...4]	
Fan Voltage	12V 5V	Selects the fan voltage. (only possible with premium fan hardware solution)

Baseboard Hardware Health

Advanced		BIOS SETUP UTILITY	
BaseBoard Hardware Health Configuration		Enables Hardware Health Monitoring Device.	
H/W Health Function	[Enabled]		
Hardware Health Event Monitoring		← Select Screen ↑↓ Select Item +− Change Option F1 General Help F10 Save and Exit ESC Exit	
Temperature Sensor #1	:123°C/253°F		
Temperature Sensor #2	:123°C/253°F		
Temperature Sensor #3	:123°C/253°F		
VcoreA	:0.048 V		
VcoreB	:0.048 V		
+3.3Vin	:0.048 V		
+5V regular	:5.214 V		
+12Vin	:0.182 V		
−12Vin	−14.667 V		
−5Vin	−7.563 V		
+5V standby	:5.213 V		
v02.61 (C)Copyright 1985–2006, American Megatrends, Inc.			

Feature	Option	Description
H/W Health Function	Disabled Enabled	Enables Hardware Health Monitoring Device.

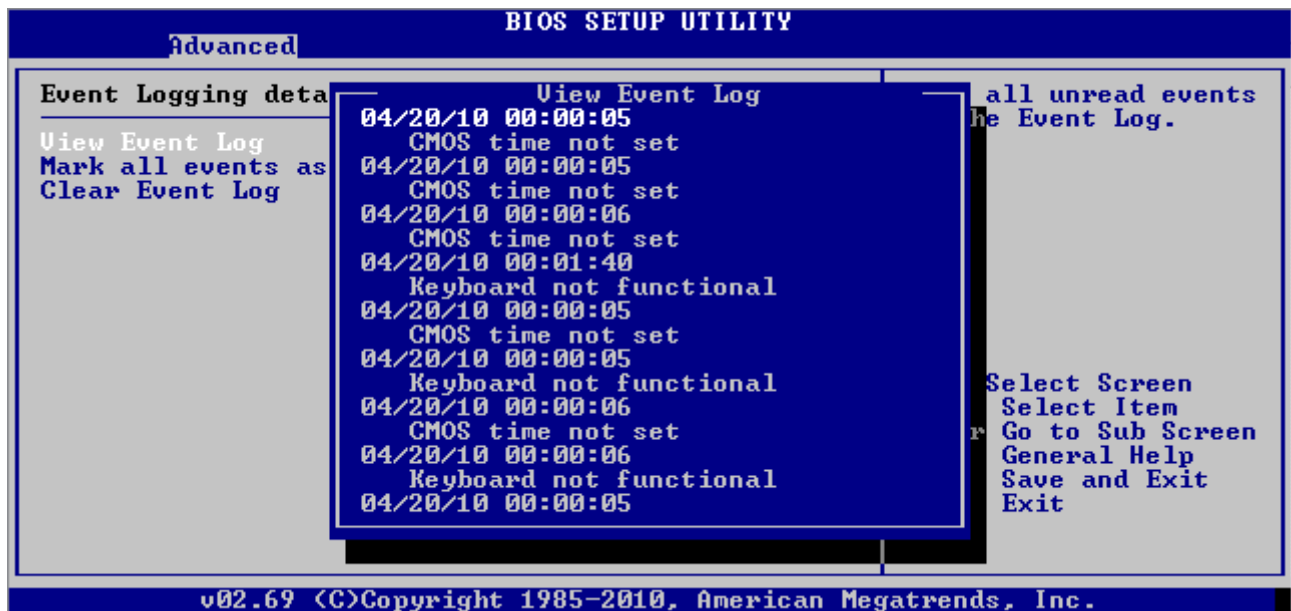
Miscellaneous Settings

Advanced		BIOS SETUP UTILITY			
Miscellaneous Settings		Mark as read, Clear or View Event Log statistics.			
▶ Event Log Configuration Post User Delay [1 Sec] Restore on AC Power Loss [Power On] Power Up Delay [Disabled] On Reset [Chipset Reset] Standby Voltage [Auto] Keyboard Crisis Recovery [Enabled] S5 Eco [Disabled]					
▶ MARS Interface Configuration ▶ Watchdog ▶ I2C Buses ▶ Remote Access Configuration ▶ Ethernet Configuration		← Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit			
v02.69 (C)Copyright 1985–2010, American Megatrends, Inc.					

Feature	Option	Description
Post User Delay	None 1 Sec 2 Sec ... 10 Min	Delay during POST
Restore on AC Power Loss	Power Off Power On	Controls the behavior after Power Loss in ATX mode
Power Up Delay	Disabled 4 to 5 seconds	Delay after power up, when in an G3 cycle

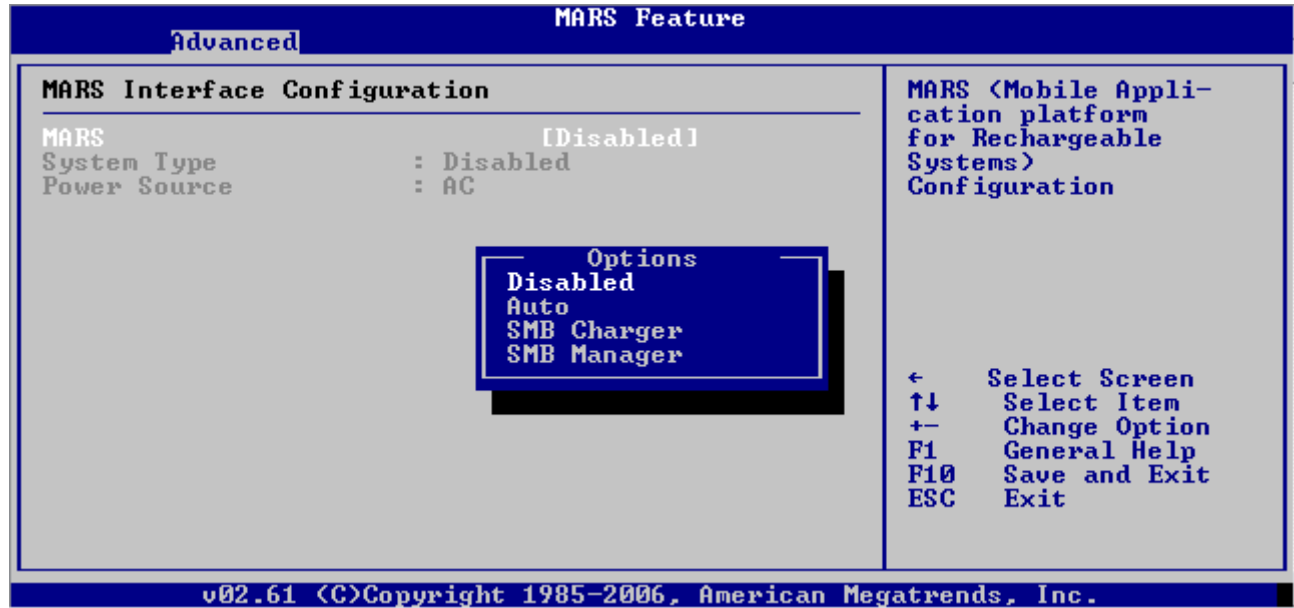
	3 to 4 seconds 2 to 3 seconds 1 to 2 seconds	
On Reset	Chipset Reset Power Cycle	Controls the behavior in reset case.
Standby Voltage	5V Standby Auto	Select which voltage is used for standby power. If using a standard ATX power supply, select 5V.
Keyboard Crisis Recovery	Disabled Enabled	Enables/Disables Keyboard Crisis Recovery function by USB keyboard
S5 Eco	Disabled Enabled	Enables/Disables S5 Eco Mode to reduce supply current in soft off (S5). See manual for usage of S5 Eco.

Event Log Configuration



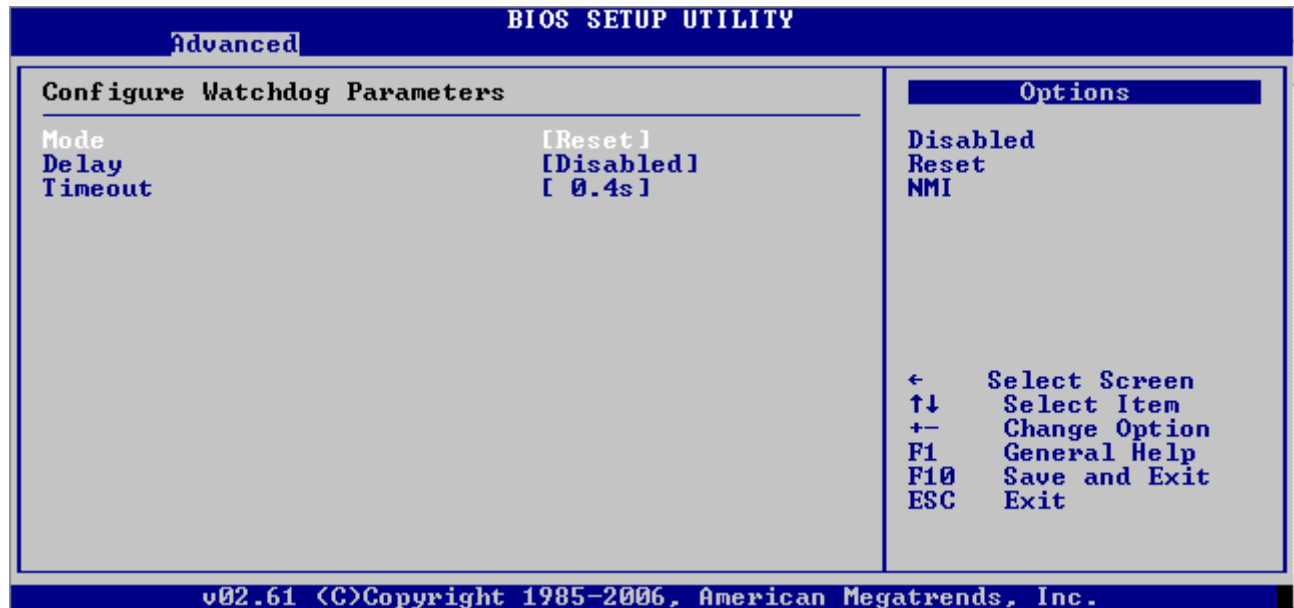
Feature	Option	Description
View Event Log		View All Unread Events in the Event Log
Mark all events as read		Mark All Unread Events as read
Clear Event Log		Discard All Unread Events in the Event Log

MARS Interface Configuration



Feature	Option	Description
MARS	Disabled Auto SMB Charger SMB Manager	Enables the MARS function

Watchdog



Feature	Option	Description
Mode	Reset Disabled NMI	Selects the mode of the watchdog
Delay	Disabled 1s	Controls the delay after the watchdog is initialized

	5s 10s 30s 1:00m 5:00m 10:00m 30:00m	
Timeout	0.4s 1s 5s 10s 30s 1:00m 5:00m 10:00m	Set the timeout for Watchdog

I2C Busses

BIOS SETUP UTILITY

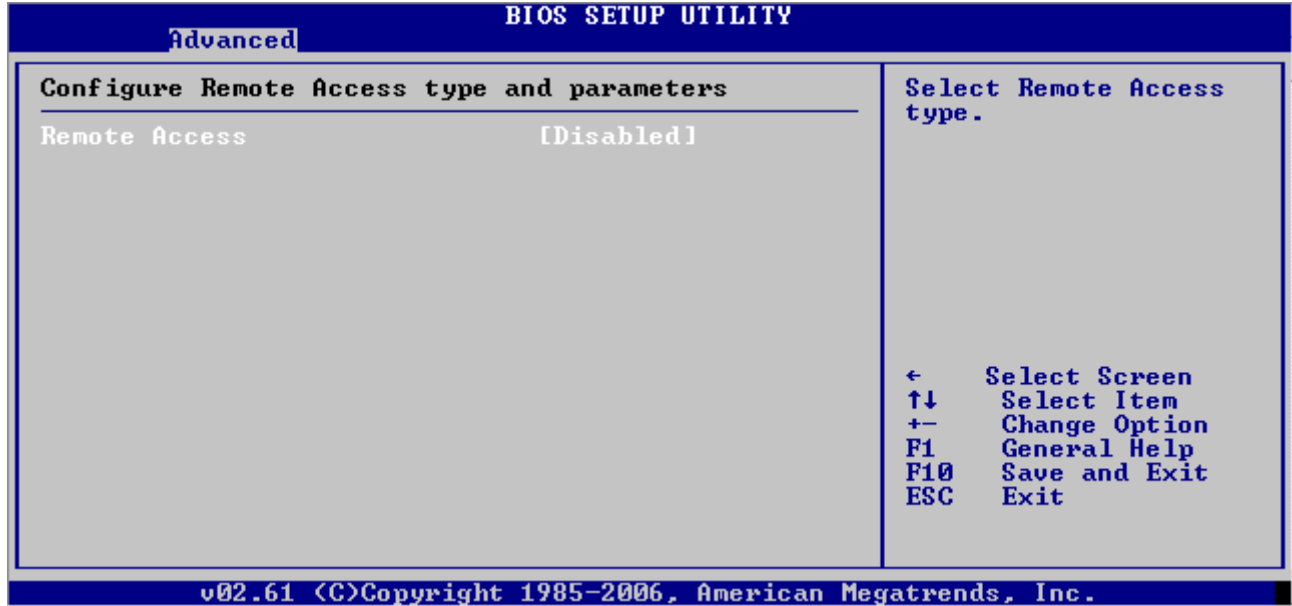
Advanced

i2C Bus Configuration	Options
External I2C Bus Speed [400Khz]	800Khz 400Khz 200Khz 100Khz 50Khz 25Khz 12Khz 6Khz 3Khz ← Select Screen ↑↓ Select Item +− Change Option F1 General Help F10 Save and Exit ESC Exit

v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

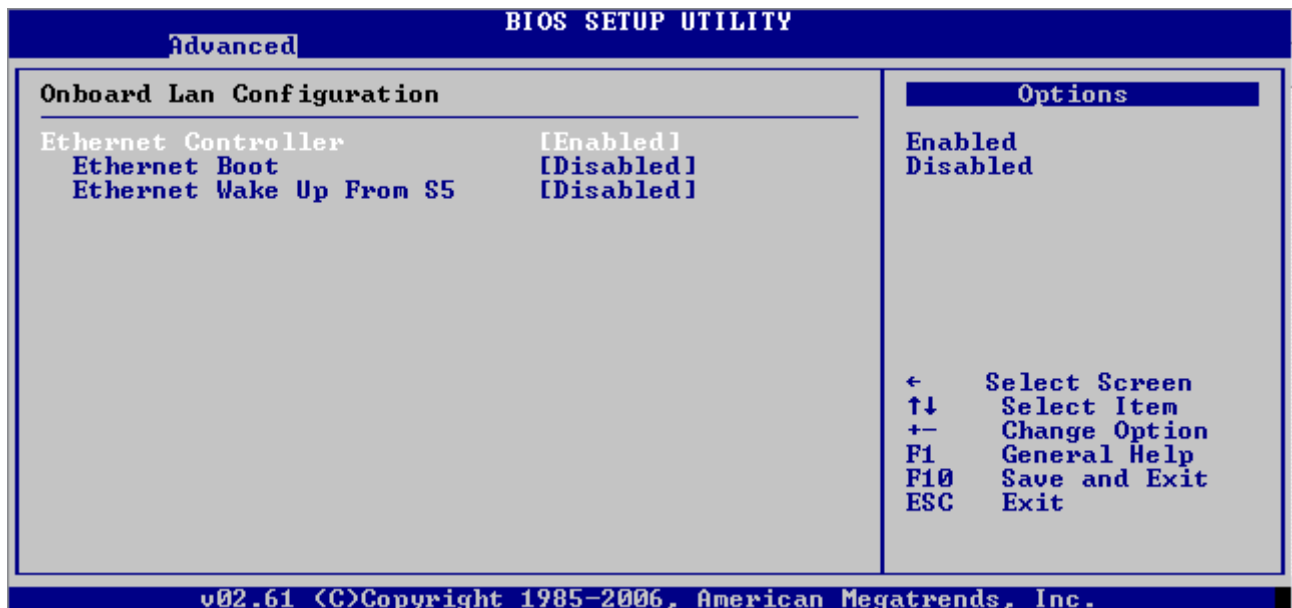
Feature	Option	Description
External I2C Bus Speed	800Khz	Controls the Bus Speed of the external I2C bus
	400Khz	
	200Khz	
	... 3Khz	

Remote Access Configuration



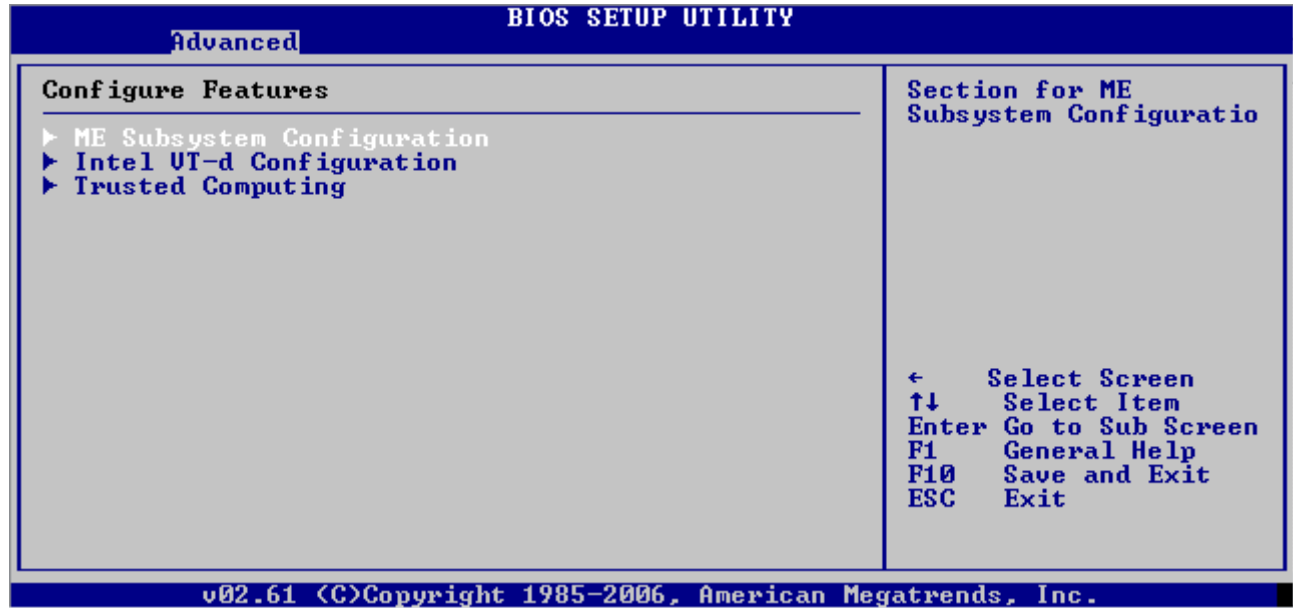
Feature	Option	Description
Remote Access	Enabled Disabled	Enables Remote Access via AMI Console Redirection

Ethernet Configuration

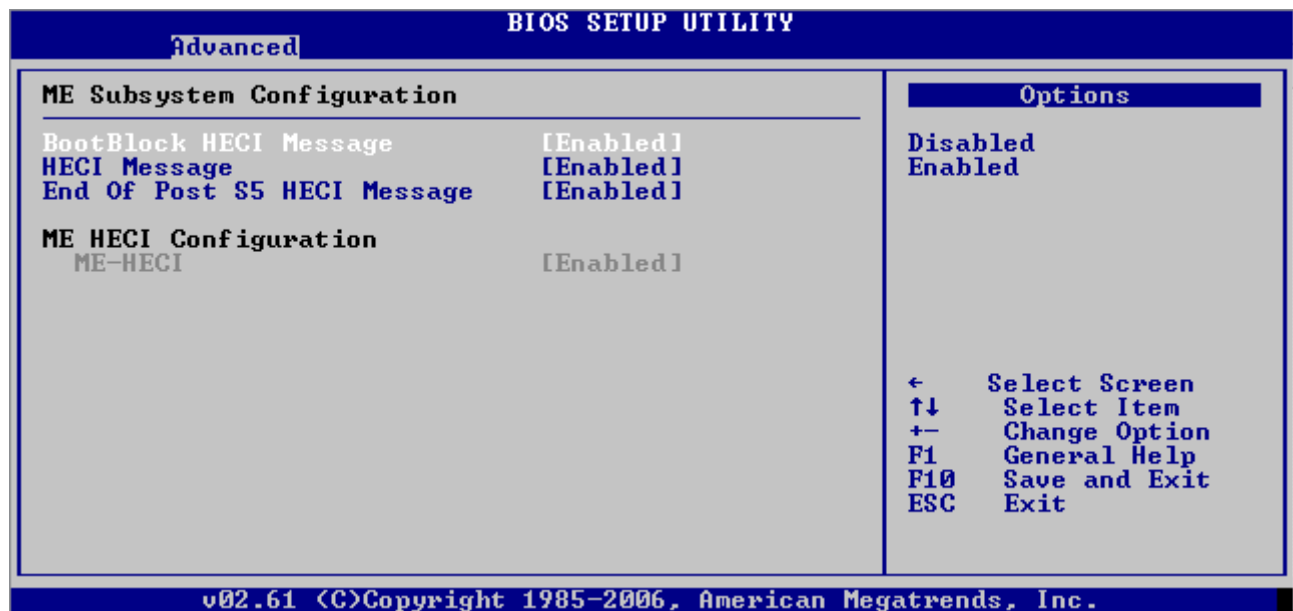


Feature	Option	Description
GbE LAN	Disabled Enabled	Disables / Enables the onboard Ethernet interface
GbE LAN Boot	Disabled Enabled	Disables / Enables the PXE Boot ROM
GbE Wake Up From S5	Disabled Enabled	Disables / Enables the WOL function from S5 ACPI state

Features



ME Subsystem Configuration



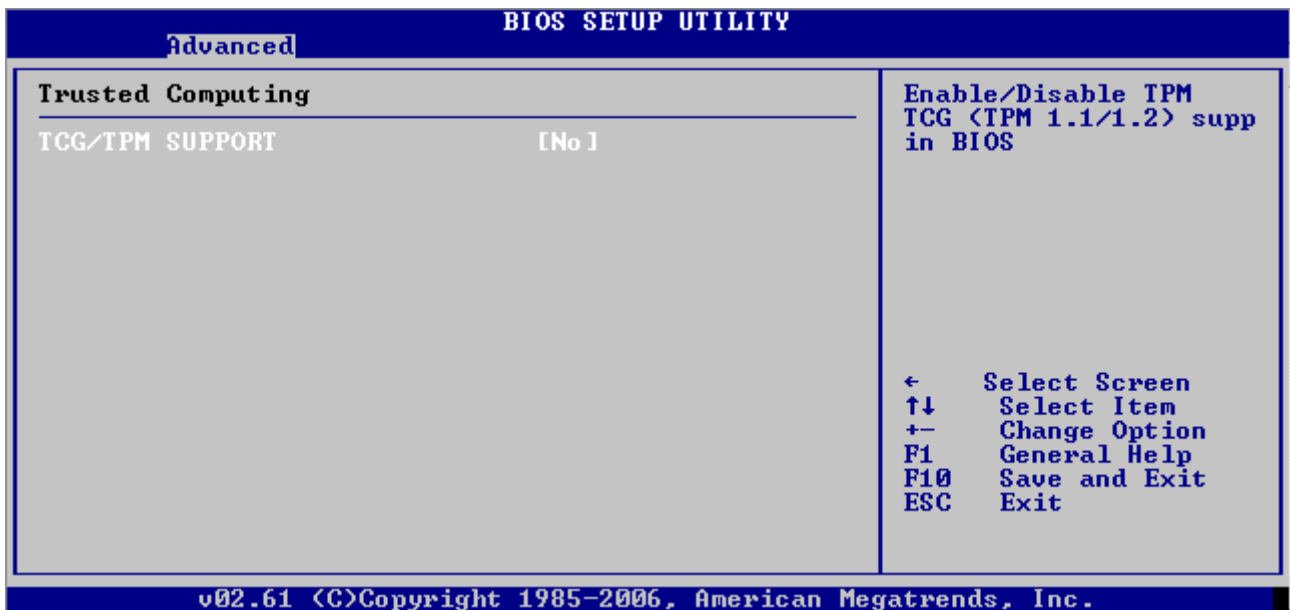
Feature	Option	Description
BootBlock HECI Message	Enabled Disabled	Selects the mode of the watchdog
HECI Message	Enabled Disabled	Enables / Disables the HECI Message
End of Post S5 HECI Message	Enabled Disabled	
ME-HECI	Enabled Disabled	

Intel VT-d Configuration



Feature	Option	Description
Intel VT-d	Enabled Disable d	Enables / Disables Intel Virtualisation Technology support

Trusted Computing



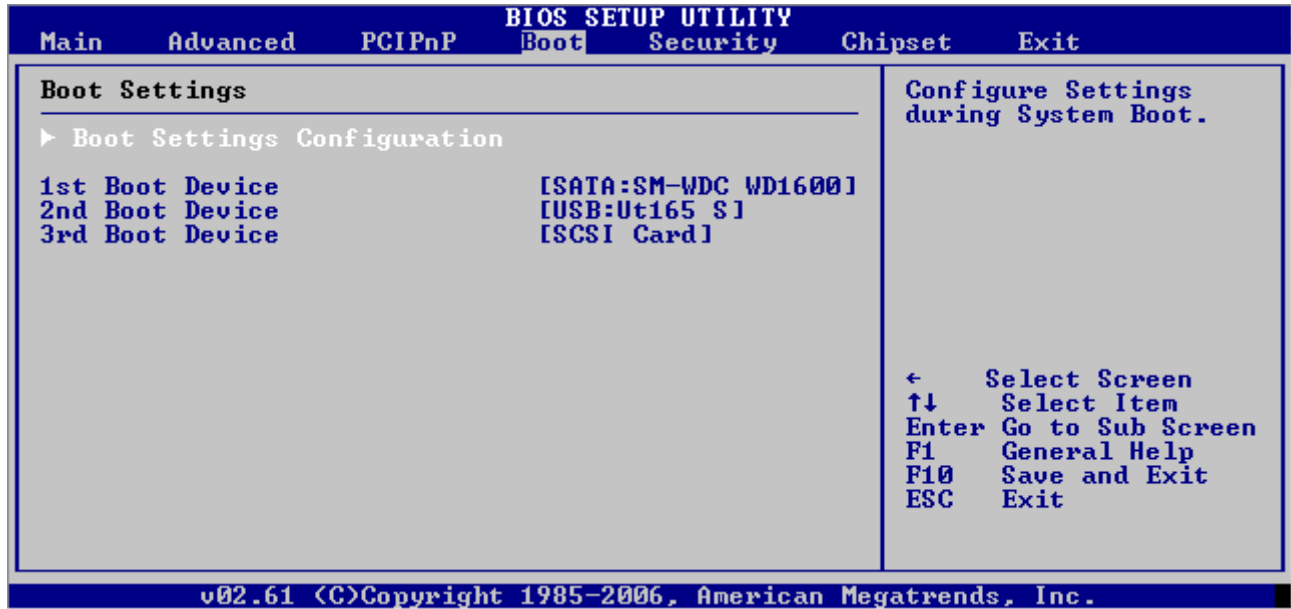
Feature	Option	Description
TCG/TPM Support	Yes No	Enables / Disables Trusted Computing and Trusted Platform Module

8.3.4 PCIPnP Menu

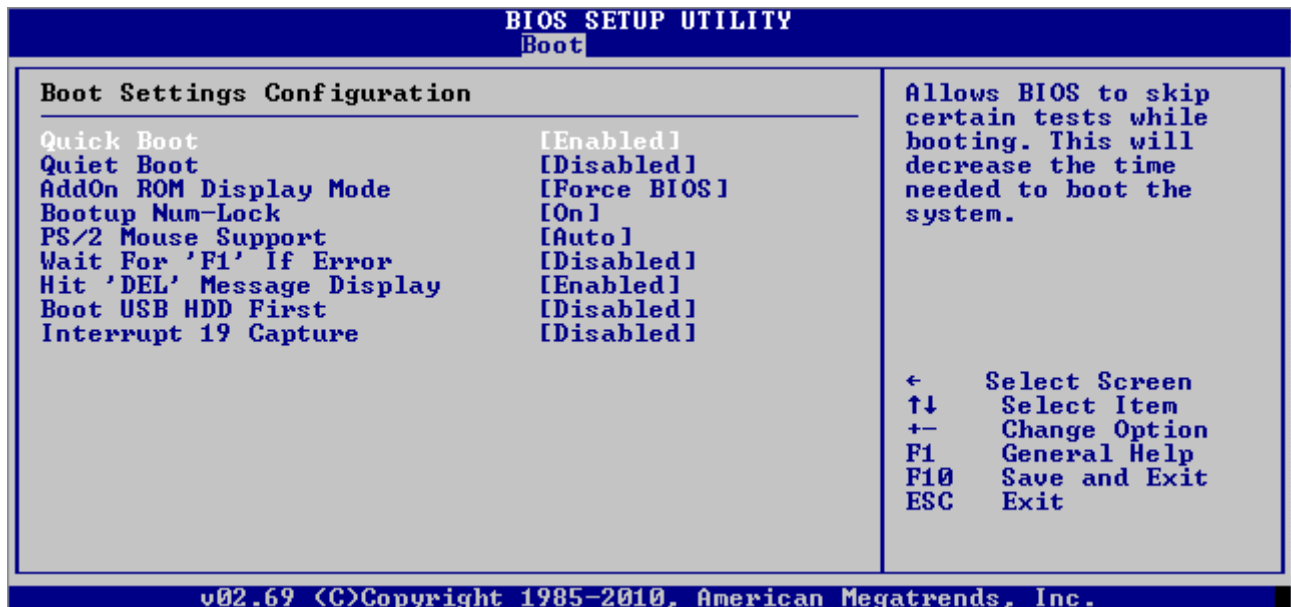
BIOS SETUP UTILITY						
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
Advanced PCI/PnP Settings WARNING: Setting wrong values in below sections may cause system to malfunction.					Clear NURAM during System Boot.	
Clear NURAM [No] Plug & Play O/S [No] PCI Latency Timer [64] Allocate IRQ to PCI VGA [Yes] Palette Snooping [Disabled] PCI IDE BusMaster [Enabled] OffBoard PCI/ISA IDE Card [Auto]						
IRQ3 [Available] IRQ4 [Available] IRQ5 [Available] IRQ7 [Available] IRQ9 [Available] IRQ10 [Available] IRQ11 [Available] IRQ14 [Available] IRQ15 [Available]						
DMA Channel 0 [Available] DMA Channel 1 [Available] DMA Channel 3 [Available] DMA Channel 5 [Available] DMA Channel 6 [Available] DMA Channel 7 [Available]						
					← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit	
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.						

Feature	Option	Description
Clear NVRAM	No Yes	Clear NVRAM once during next system boot.
Plug & Play O/S	No Yes	No: all devices are initialized by BIOS Yes: OS has to initialize some devices
PCI Latency Timer	32 64 ... 248	Value in units of PCI clocks for PCI device latency register
Allocate IRQ to PCI VGA	Yes No	Decided if PCI VGA card does get an IRQ assigned if requested
Palette Snooping	Disabled Enabled	Disables and enables Palette Snooping
PCI IDE BusMaster	Disabled Enabled	Disables and enables PCI IDE Busmaster
OffBoard PCI/ISA IDE Card	Auto PCISlot 1 PCISlot 2 ... PCISlot 6	Some IDE Cards needs this , with set to Auto it works with most cards
IRQ3 ... IRQ15	Available Reserved	Available: IRQ useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices
DMA Channel 0 ... DMA Channel 7	Available Reserved	Available: DMA useable by PCI/PnP devices Reserved: IRQ is reserved for ISA devices

8.3.5 Boot



Boot Setting Configuration



Feature	Option	Description
Quick Boot	Enabled Disabled	Disables or enables the quick boot feature
Quiet Boot	Disabled Enabled	Disabled: Shows normal POST messages Enabled: Shows OEM Logo during boot up
AddOn ROM Display Mode	Force BIOS Keep Current	Set Display Mode for Option ROM
Bootup Num-Lock	On Off	Select Power-On state for Num-Lock
PS/2 Mouse Support	Auto Disabled Enabled	Disables and enables or auto selects PS/2 Mouse Support

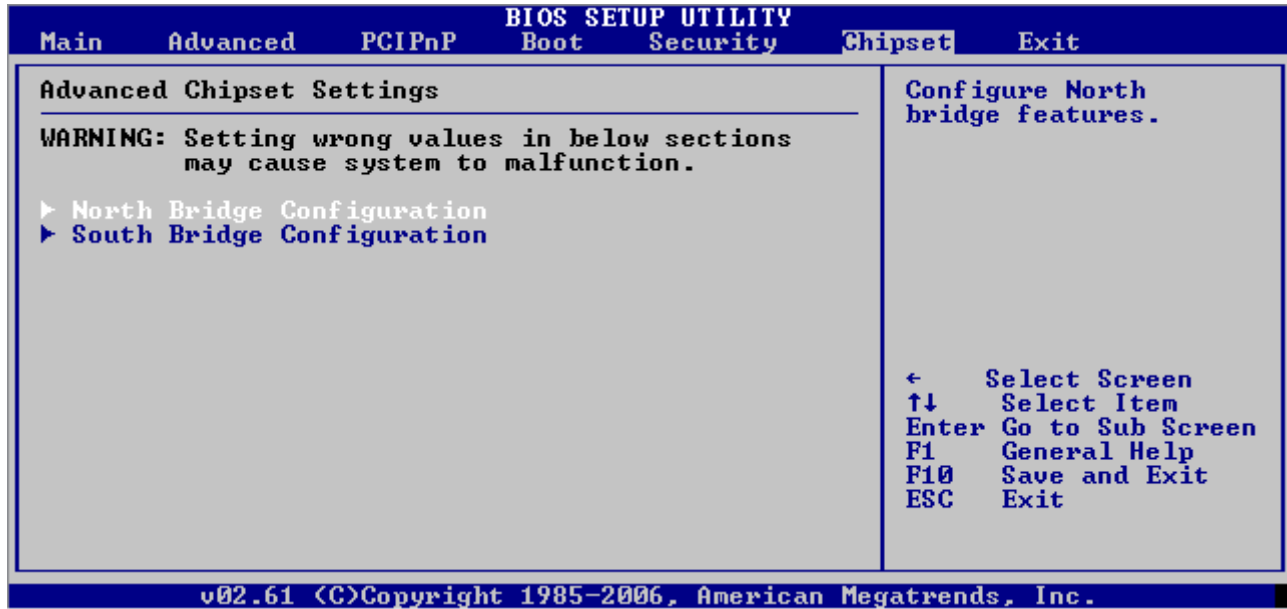
Wait For 'F1' If Error	Disabled Enabled	Wait for F1 key to be pressed, if error
Hit 'DEL' Message Display	Enabled Disabled	Displays: „Hit 'DEL' to run setup“ during POST, if enabled
Boot USB HDD first	Disabled Enabled	If enabled, boots new attached USB HDD always first. If disabled, sets new attached USB HDD to last boot position
Interrupt 19 Capture	Disabled Enabled	Allows option ROMs to trap INT19h if enabled

8.3.6 Security

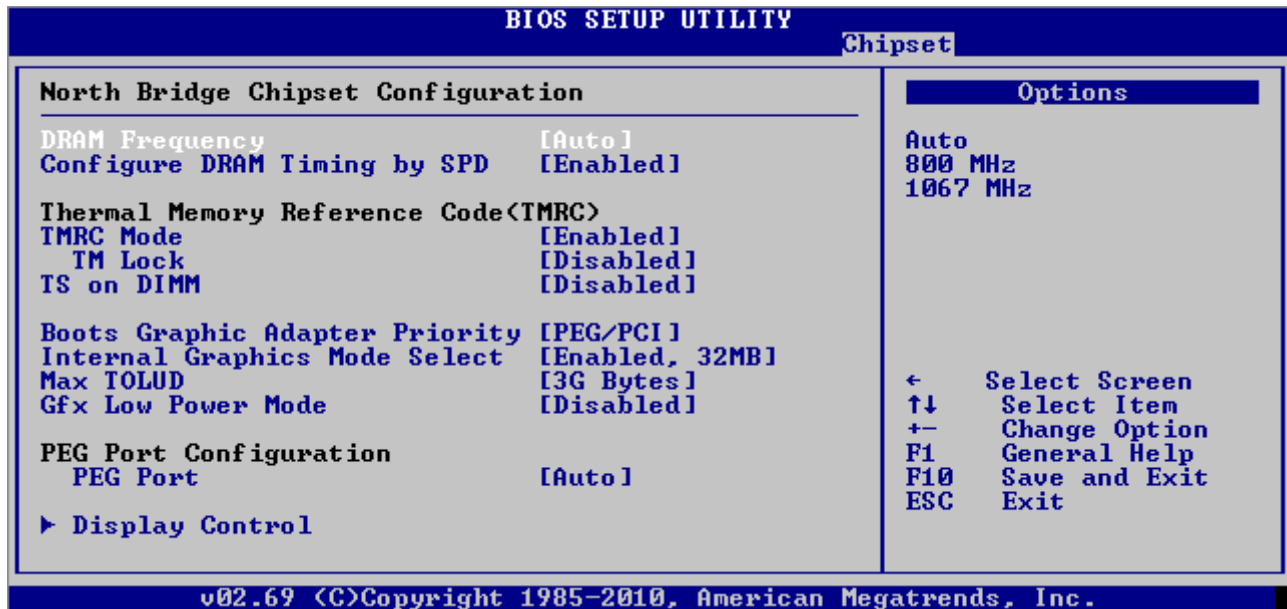
BIOS SETUP UTILITY	
Main	Advanced
Security Settings <hr/> Supervisor Password :Not Installed User Password :Not Installed Change Supervisor Password Change User Password Boot Sector Virus Protection [Disabled] Hard Disk Security <hr/> Secondary Master HDD Password Status :Disabled <hr/> Secondary Master HDD User Password	Install or Change the password. ← Select Screen ↑↓ Select Item Enter Change F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

Feature	Option	Description
Change Supervisor Password	Type in	
Change User Password	Type in	
Boot Sector Virus Protection	Disabled Enabled	Enables or disables boot sector virus protection.

8.3.7 Chipset



North Bridge Configuration



Feature	Option	Description
DRAM Frequency	Auto 800Mhz 1067Mhz	Selects the DRAM frequency
Configure DRAM Timing by SPD	Disabled Enabled	Disables and Enables automatic DRAM configuration via SPD EEPROM
TMRC Mode	Disabled Enabled	Disables and Enables the thermal memory reference code.
TM Lock	Disabled Enabled	Disables and Enables the Thermal Sensor on Lock.
TS on DIMM	Disabled Enabled	Disables and Enables the Thermal Sensor on DIMM.
Boots Graphic Adapter Priority	IGD	Selects which graphics adapter is initialized during boot up and

	PCI/IGD PCI/PEG PEG/IGD PEG/PCI	gets priority
Internal Graphics Mode Select	Disabled Enabled, 32MB Enabled, 64MB Enabled, 128MB	Select the mode for the internal graphic device
Max TOLUD	3G Bytes 2.5G Bytes 2G Bytes	Maximum value of „top of low usable DRAM“
Gfx Low Power Mode	Disabled Enabled	Disables and Enables the low power mode for the internal graphics device
PEG Port	Auto Disabled Enable PEG Port Always	Selects the initialization mode of the PCIexpress graphics port

Display Control

```

BIOS SETUP UTILITY
Chipset
-----
JDA Revision      : 1.11
UBIOS Revision   : 1744
JILI Core Revision : 1.1.1

DVTM/FIXED Memory [256MB]
PAVP Mode         [Disabled]
Boot Display Device [CRT + LVDS]
▶ Internal LVDS Configuration
TV Standard      [NTSC]
TV Sub-Type      [NTSC-M]
HDMI DP Support  [Disabled]
HDCP Support     [Disabled]

← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit

v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.
    
```

Feature	Option	Description
DVMT/FIXED Memory	128MB 256MB \\Max DVMT	Configures the amount of memory for the Dynamic Video Memory Technology
PAVP Mode	Disabled Light High	Configures the Protected Audio Video Path
Boot Display Device	CRT TV SDVO CRT+SDVO LVDS CRT+LVDS	Selects the Boot Display Devices

TV Standard	NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Selects the regarding TV standard for TV out interface
TV Sub-Type	Depending on TV Standard	Selects the regarding TV Sub-Type
HDMI DP Support	Disabled Enabled	Enables and disables the HDMI DP Support
HDCP Support	Disabled Enabled	Enables and disables the HDCP Support

Internal LVDS Configuration

Chipset	
Current LVDS Configuration Data Source : NONE Resolution : N/A Color Depth : N/A Channel Count : N/A Dithering : N/A Flat Panel Mode [Fixed Mode] Flat Panel Type [XGA 1024x768] PAID/FPID [5] Channels [Single Channel] Color Depth [18Bit] Local Flat Panel Scaling [Stretched] Backlight Control Type [I2C] Backlight Brightness [128]	Options Single Channel Dual Channel ← Select Screen ↑↓ Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.	

Feature	Option	Description
Flat Panel Mode	Auto Fixed Mode PAID FPID	Selects the Mode for the flat panel detection
Auto Fallback	Disabled Fixed Mode	Selects what happens, when there is no EEPROM detected (only when FPM: Auto)
Flat Panel Type	VGA 640x480 ... WXGA 1280x800	Selects the resolution of the LVDS display (only in FMP: Fixed Mode)
PAID/FPID	[X]	Selects the number of the PAID/FPID
Channels	Single Channel Dual Channel	Selects, if 1x or 2x LVDS signals are used (only in FPM: Fixed Mode)
Color Depth	18bit 24bit open LDI 24bit	Selects the Color Depth of the connected LVDS display (only in FPM: Fixed Mode)
Local Flat Panel Scaling	Centered Stretched	Selects the Scaling Options for the LVDS panel (only in FPM: Fixed Mode)

	Disabled	
Backlight Control Type	None/External I2C PWM	Selects the mode for Backlight Control
Backlight Brightness	[0...255]	Selects the default setting for Backlight Brightness

Southbridge Configuration

BIOS SETUP UTILITY **Chipset**

South Bridge Configuration

USB Functions [8 USB Ports + IDE]
USB Port Configure [6+4 USB Ports]
 USB 2.0 Controller [Enabled]

Enable Lock Bit [Enabled]
 Port 80h Output [LPC]
 Audio Controller [Enabled]
 SMBUS Controller [Enabled]

▶ LPC Decode Range

Enable/disable USB ports.

Note:
 The parallel ATA channel is hosted by an USB2ATA bridge at the 9th USB port. Disabling this port will also disable parallel ATA!

← Select Screen
 ↑↓ Select Item
 +- Change Option
 F1 General Help
 F10 Save and Exit
 ESC Exit

v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

Feature	Option	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports ... 8 USB Ports + IDE	Enables / Disables USB ports*
USB Port Configure	6+4 USB Ports 8+2 USB Ports	Configures, how the ports are mapped internally to the USB controllers
USB 2.0 Controller	Enabled Disabled	Enables / Disables the USB 2.0 controller. (only available when there is USB2ATA port disabled)
Enable Lock Bit	Disabled Enabled	Enables Lock bit at end of POST. Only disable for debugging purposes.
Port 80h Output	LPC PCI	Selects the Interface for Port 80h output during POST
Audio Controller	Enabled Disabled	Enables / Disables the HDA audio controller
SMBUS Controller	Enabled Disabled	Enables / Disables the SMBus controller



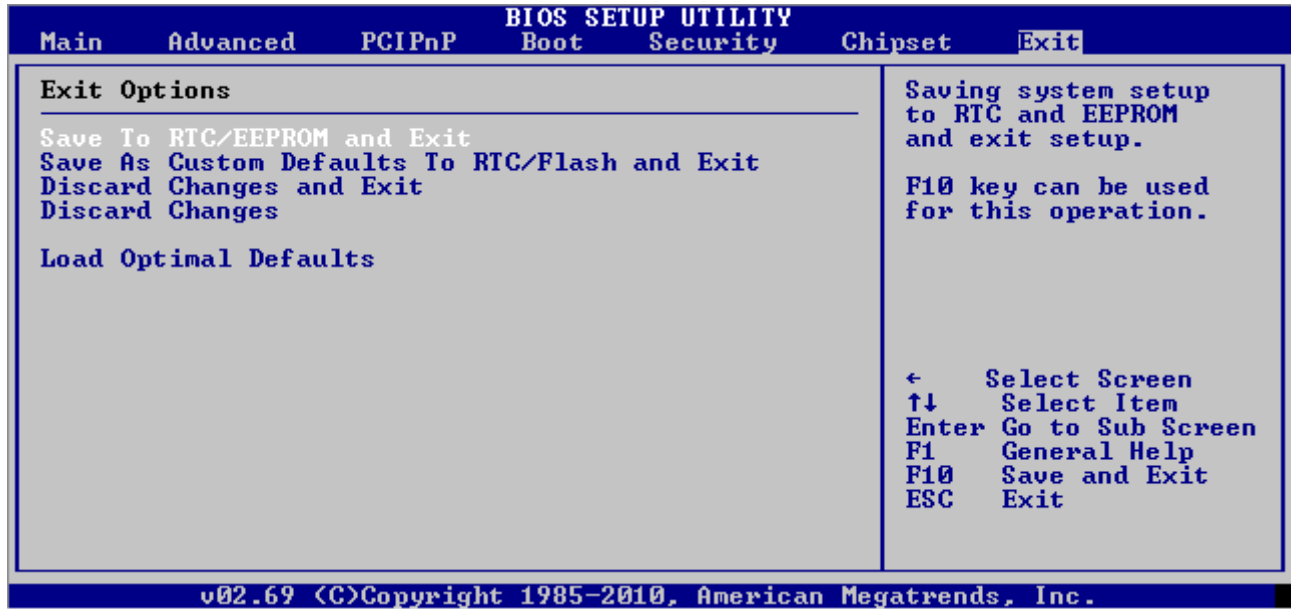
* The parallel ATA channel is hosted by an USB2PATA bridge at the 9th USB port. Disabling this port will also disable parallel ATA!

LPC Decode Range

BIOS SETUP UTILITY		Chipset
LPC Decode Range		Enable the range to be forwarded to the LPC I/F ← Select Screen ↑↓ Select Item Enter Update F1 General Help F10 Save and Exit ESC Exit
LPC Decode Range 1 Base	[0]	
LPC Decode Range 1 Size	[Disabled]	
LPC Decode Range 2 Base	[0]	
LPC Decode Range 2 Size	[Disabled]	
LPC Decode Range 3 Base	[0]	
LPC Decode Range 3 Size	[Disabled]	
LPC Decode Range 4Eh/4Fh	[Enabled]	
LPC Decode Range 62h/66h	[Disabled]	
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.		

Feature	Option	Description
LPC Decode Range 1 Base	[0...FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 1 Size	Disabled 4 8 ... 256	Size of the decode range in kB
LPC Decode Range 2 Base	[0...FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 2 Size	Disabled 4 8 ... 256	Size of the decode range in kB
LPC Decode Range 3 Base	[0...FFFF]	Enter the Base Adress of the LPC decode range
LPC Decode Range 3 Size	Disabled 4 8 ... 256	Size of the decode range in kB
LPC Decode Range 4Eh/4Fh	Enabled Disabled	Enables disables the LPC decode range at 4Eh/4Fh
LPC Decode Range 62h/	Disabled Enabled	Enables disables the LPC decode range at 62h/66h

8.3.8 Exit Menu



9 Document Revision History

Revision	Date	Edited by	Changes
001	22.06.09	UMA	Preliminary Release
100	17.02.10	UMA	Corrected typos, added power measurements, removed heatspreader drawing, mentioned x4 PCIe, updated fan connector description, fan BIOS settings, fan electrical characteristics, added mechanical measurements, added BIOS setup description of CNTGR413 which should be 99% accurate
1.1	29.06.10	UMA	switched to new documentation system, added flash backup, dynamic FSB frequency switching, enhanced Intel dynamic acceleration and vid-x, removed appendices, updated BIOS description to UNTGR410

Corporate Offices

Europe, Middle East & Africa	North America	Asia Pacific
Oskar-von-Miller-Str. 1 85386 Eching/Munich Germany Tel.: +49 (0)8165/ 77 777 Fax: +49 (0)8165/ 77 219 info@kontron.com	14118 Stowe Drive Poway, CA 92064-7147 USA Tel.: +1 888 294 4558 Fax: +1 858 677 0898 info@us.kontron.com	17 Building,Block #1,ABP. 188 Southern West 4th Ring Beijing 100070, P.R.China Tel.: + 86 10 63751188 Fax: + 86 10 83682438 info@kontron.cn

